Fabrication of Sub-10 nm Metal Wire Circuits using Directed Self-Assembly of Block Copolymers


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A novel half-pitch (HP) 10 nm physical-epitaxial frequency multiplication process using a high chi (χ) lamellar block copolymer was developed to carry out process verification of directed self-assembly lithography on a 300 mm wafer for practical semiconductor device manufacturing. Electrically open and short process level-test element group (PL-TEG) yield verification of sub-10 nm metal wire circuits fabricated using the HP 10 nm physical-epitaxial frequency multiplication process was carried out on a 300 mm wafer. The electrically open and short PL-TEG yield verification revealed the viability of the HP 10 nm physical-epitaxial frequency multiplication process from the perspective of the total practical performance including critical dimension control, defect control, pattern placement error, space width roughness, space edge roughness, and process windows in the pattern transfer process.

Keywords: lithography, sub-10 nm, metal wire circuit, directed self-assembly, block copolymer

1. Introduction

Directed self-assembly (DSA) of block copolymers (BCPs) has been expected as a potential complimentary lithographic technique for frequency multiplication processes towards half pitches (HPs) below 10 nm patterns. There have ever been reported several frequency multiplication processes with polystyrene-block-poly(methyl methacrylate) (PS-\(b\)-PMMA) lamellar BCPs such as SMART™ flow [1] and LiNe flow [2]. We have also demonstrated electrical yield verification of HP 15 nm metal wire circuits fabricated using a novel frequency multiplication, “COOrdinated Line epitaxy (COOL) process”, with the lamellar PS-\(b\)-PMMA [3-6]. However, further scaling with the lamellar PS-\(b\)-PMMA towards HPs below 10 nm patterns is strictly limited because of a relatively low Flory-Huggins interaction parameter, \(\chi\) (chi), between PS and PMMA blocks.

In this work, we demonstrated electrical yield verification of sub-10 nm metal wire circuits fabricated using a physical-epitaxial frequency multiplication process with a combination of neutral layer and high chi (χ) lamellar BCP, in order to open a breach in the further scaling towards HPs below 10 nm patterns [7-10]. The electrical process level-test element group (PL-TEG) yield could reveal the process viability from the perspective of totally practical performance for semiconductor device manufacturing including critical dimension (CD) control, defect control, pattern placement error, space width roughness (SWR), space edge roughness (SER), and process windows in pattern transfer process [6,11,12].

2. Experimental

The HP 10 nm physical-epitaxial frequency multiplication process steps using the high \(\chi\) lamellar BCP are shown in Fig. 1. First of all, 45 nm line and 55 nm space resist patterns to fabricate
guide patterns were exposed on a spin-on-glass (SOG), spin-on-carbon (SOC), SiO$_2$, amorphous silicon (a-Si), SiO$_2$ stacked silicon substrate on a 1.3 numerical aperture (NA) ArF excimer laser immersion scanner (NSR S610C, Nikon Corp.). The SiO$_2$ guide patterns were then fabricated using the resist patterns on the SOG and the SOC [13-16] on a dry etcher (Tactras SCCM-T4, Tokyo Electron Ltd.). A random BCP solution as a neutral layer was then grafted and a high $\chi$ lamellar BCP solution with 20 nm $L_0$ (domain spacing) was applied on the SiO$_2$ guide patterns using a Clean Track ACT12 (Tokyo Electron Ltd.). Finally, the HP 10 nm physical-epitaxial frequency multiplication patterns were fabricated after removing one of a pair segment on the dry etcher. That is, two HP 10 nm space patterns are located in between the physical guide patterns.

[Image of HP 10 nm physical epitaxy process]

Fig. 1. HP 10 nm physical epitaxy process.

Defect inspection and classification were performed to effectively improve the DSA defects on an electron beam (EB) defect inspection system (NGR3250, NGR Inc.) [17, 18]. Next, critical dimension (CD), space width roughness (SWR), space edge roughness (SER), local placement error, and power spectral density (PSD) were measured on a critical dimension-scanning electron microscope (CD-SEM) (CG5000, Hitachi High-Technologies Corp.) [19,20]. Electron beam absorbed current (EBAC) system [21, 22,23], transmission electron microscopy (TEM), and scanning transmission electron microscopy (STEM) were performed to conduct failure analysis capable of physically and electrically analyzing the DSA defects in the sub-10 nm metal wire circuits.

3. Results and Discussion

DSA defect classification after dry development was demonstrated using NGR3250 as shown in Fig. 2. The DSA defect inspection area was 0.22 mm$^2$. It was found that major DSA defects were single short, multi-short and half short. There observed neither dislocation defects nor disclination defects in this experiment.

[Image of DSA defect classification]

Fig. 2. DSA defect classification.

CD data analyses in the HP 10 nm physical epitaxy process were carried out using CG5000 as shown in Fig.3. It was found that the space width CD was approximately 9 nm, and that the SWR was less than 2 nm, and that space placement error was less than 2 nm, respectively. These values have to be reduced to a level of less than 1.0 nm for practical semiconductor device manufacturing using HP sub-10 nm patterning. It was found that the SER adjacent to isolated line patterns was by 0.2 nm smaller than that adjacent to the physical guide patterns. It is considered to be due to DSA smoothing effects. The properties of the physical guide patterns could be important factors in reducing the SWR and the SER. The PSD revealed approximately 50 - 100 nm pitch peak possibly due to guide pattern roughness and approximately 25 nm pitch peak possibly due to short defects, so called the grid defects [3-7, 24].

Process flows for electrical PL-TEG yield verification using a combination of the physical-epitaxial frequency multiplication process and damascene process [25] are shown in Fig. 4. The combined process comprises a set of four ArF laser immersion scanner exposures for alignment mark patterns as the 0th layer, the physical guide
patterns as the 1st layer, connect patterns as the 2nd layer and cut patterns as the 3rd layer.

Figure 5 shows cross-sectional SEM profiles of HP 10 nm open and short PL-TEG circuits after cut exposure and etch in Fig. 4. They show that HP 10 nm open and short PL-TEG circuit patterns were successfully fabricated using the combined process without the use of any multi-patterning, such as self-aligned quadruple patterning [26-28].

Figure 6 shows cross-sectional STEM profiles of metal wire circuits with 9 nm in width after metal deposition and chemical mechanical polishing (CMP). They show that the metal wire circuits with 9 nm in width were successfully fabricated using the combined process.

The HP 10 nm open and short PL-TEG circuit layout on 300 mm wafer is shown in Fig. 7. The layout has a variety of open and short PL-TEG circuits at 142 sites for each shot. In this experiment, out of the total 295 shots, 87 shots around the wafer center were electrically measurable. The HP 10 nm open and short PL-TEG yield data of the metal wire circuits with 700 µm in length could electrically be verified in few sites.

Figure 8 shows physical failure analysis of the metal wire circuits with 9 nm in width using EBAC system. Because the electrically open and short PL-TEG yield was still relatively low for the practical semiconductor device manufacturing using the DSA of BCPs, the EBAC analysis was carried out to investigate the cause of the electrical failure. The EBAC analysis could determine line breaking points of the metal wire line patterns with
9 nm in width. Electrical failure analysis is capable of physically and electrically analyzing the defects that will make a valuable contribution to the electrical open and short PL-TEG yield. The EBAC system revealed the line breaking with approximately 25 nm in length on the metal wire line pattern with 9 nm in width. It is considered that the line breaking was caused by the short defect, so called the grid defect [29-33].

Figure 9 shows defect classification of the metal wire circuits with 9 nm in width. The EBAC system did not find any line breaking defects in SUCCESS site. On the other, it found a line breaking defect with approximately 50 nm in length, which is possibly due to the physical guide pattern roughness as shown in Fig. 3, in FAIL site.

4. Conclusion
The novel HP 10 nm physical-epitaxial frequency multiplication process using the high $\chi$ lamellar BCP with 20 nm L_0 was developed to carry out process verification of the DSA lithography on the 300 mm wafer for the practical semiconductor device manufacturing. The electrically open and short PL-TEG yield verification of the metal wire circuits with 9 nm in width fabricated using the HP 10 nm physical-epitaxial frequency multiplication process was carried out on the 300 mm wafer. The electrically open and short PL-TEG yield verification revealed the viability of the HP 10 nm physical-epitaxial frequency multiplication process from the perspective of the total practical performance including the CD control, the defect control, pattern placement error, the SWR, the SER, and the process window in the pattern transfer process.

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References
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