Defectivity Study for Directed Self-Assembly (DSA) Contact Hole Shrink

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Directed Self-Assembly (DSA) is one of the candidates for scaling feature sizes beyond 10 nm node. DSA has shown the capability for pitch reduction, contact hole (CH) shrinks and improvement in pattern profile and pattern collapse margin. Defectivity is one of the critical criteria for implementation of DSA as a technically viable approach. However, only few defectivity studies of DSA shrink in various topography have been reported. In this paper, we investigated wafer-level defectivity of DSA shrink at various stages of the DSA patterning process. The contribution from each process step and materials are partitioned and categorized. The DSA defectivity was reduced by optimizing the material quality, surface treatment and pattern transfer processes. Systematic defect sources over the wafer map have been reduced. Finally, an outlook as to the guidelines and challenges to DSA CH shrinkage process will be discussed.

Keywords: directed self-assembly, defectivity, contact hole (CH) shrinks

1. Introduction

The semiconductor integrated circuit (IC) industry has experienced exponential growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling process generally provides benefits by increasing production efficiency and lowering associated costs.

Such scaling has also increased the complexity of processing and manufacturing ICs and gradually approaches its technological and economical limits. Directed self-assembly (DSA) process emerges as a

potential candidate for patterning small and dense features by combining lithography and self-assembly polymers [1,2]. DSA process takes advantage of the self-assembling properties of materials, such as block copolymers (BCP), to reach nanoscale dimensions while meeting the constraints of current manufacturing. Defectivity is one of the keys to implement DSA in manufacturing [3-6]. In this paper, we focus on DSA defectivity study of contact hole shrinkage, and wafer-level defectivity of DSA shrink at each stage of the DSA patterning was investigated (Fig. 1). The contribution from each process step and materials are partitioned and studied using defect source analysis methodology. The DSA defectivity was reduced by optimizing the material quality, surface treatment and pattern transfer processes. Systematic defect sources over the wafer map have been reduced.

Fig. 1. Schematic of guiding pattern preparation, DSA and pattern transfer.

2. Experimental

2.1. Preparation of guiding patterns and DSA in the guiding patterns

A negative-tone imaging tri-layer stack consisting a 70 nm thick resist over 30 nm thick silicon-containing middle layer (ML) and 100 nm thick spin-on carbon bottom layer (BL) over the oxide layer was used for printing the PR guiding-pattern and generate DSA guide pattern by transferring resist pattern into SiARC and SOC (Fig. 1A). After opening the ML and BL, the resist pattern is removed and leaving a topographical substrate which is thermally stable for DSA process (Figure 1B). The topographical substrate of via arrays with via CD of 70 nm is then modified using a surface modification materials NL-A by applying NL-A, baking at 120 °C for 2 min. A solvent rinse is then applied to remove the excess of NL-A material in order to form a thin and conformal surface modification layer on the topographical substrate (Fig. 1C). After coating, baking and rinsing, the modified topographical pattern becomes a guiding pattern for directed self-assembly. A poly(styrene-*block*-methacrylate) diblock copolymer (PS-*b*-PMMA) was spin-coated and annealed on the guiding pattern at 250 °C for 5 min (Fig. 1D) to form an single exposed, cylindrical PMMA domain in a single via guide pattern. The exposed PMMA is removed by dry etch and leaving DSA via within the guiding prepattern (Fig. 1E). Another dry etch is used to transfer DSA via pattern into the underlying oxide layer (Fig. 1F).

2.2. Defect Study

A brightfield optical inspection system (KLA 2925) is used for defect inspection and defect source identification. A suitable optics-set was selected based on knowledge-based settings depending on the design layout, defects types, noise sources and stacks of thin film at any given layer to provide sensitivity to the defect types of interest. Missing holes after PMMA removal step and after pattern transfer into oxide layer are the focus of this study. The optics-set was then verified and further optimized to maximize sensitivity to all defects of interest while suppressing potential noise sources.

3. Results and Discussion

3.1. Initial defect results and defect reduction through filtration

Three major types of defects have been observed after PMMA: fall-on defects, residue defects and missing hole defects as shown in Fig. 2A. The typical size of fall-on defects is between 30 nm to 200 nm and the particle may show sharp-angles. On the other hand, the residual defect are larger and with a typically dimension between 50 nm to 300 nm. Total fall-on and residue defects are found to be ~ 353ea / wafer (Fig. 2B). Such particle defects occur randomly across the wafers and reflected that there are particles in the formulation of neutral layer or block copolymer. Enhanced filtration using filter of smaller pore size for both block copolymer and neutral layer formulation reduced particle defects from 353 to 117 ea defect / wafer as shown in Fig. 3.

3.2. Reduction of missing hole defects

The ideal phase separation for DSA via shrink is to create a single PMMA cylindrical domain at the center of the guide pattern. 40 ea missing defects / wafer were observed in the initial defect study. The missing holes where no PMMA domain are created at the center are considered as DSA intrinsic defects and may be a result from non-ideal thermal dynamic or non-ideal kinetics of phase separation of block copolymers in the surface modified guide pattern. Therefore, filter pore size reduction has no effect on the numbers of missing hole defects (Fig. 3).

Fig. 2. Initial defect counts and defect types observed in the DSA hole shrink after PMMA removal [A: SEM images B: defect count].

Fig. 3. Defect count of fall-on and residue defects are improved using formulation with enhanced filtration.

Many process tunings have been tried to reduce missing-hole defects and some of them are effective and listed in Fig. 4. One of the suspected defect root causes is that the random excess of the neutral layer may cause failure in self-assembly process. Therefore, an enhanced rinse for guiding pattern pre-clean after surface modification is employed and the defect count is reduced to 35 ea defects / wafer. In addition to the rinse, longer bake time is used to eliminate the kinetically trapped states of the borderline cases. By increasing bake time from 5 min to 10 min, missing hole defect count is reduced from 35 to 30 ea defect / wafer. It seems the interaction between neutral layer and BCP is a key factor in terms of optimization of DSA performance, by applying new brush layer, additional rinse and additional bake, the

missing defect can be reduced to 5 ea defects / wafer.

Fig. 4. Reduction of missing hole defects.

A defect monitor wafer prepared using best-known method (Fig. 5A) is then transferred into oxide layer (Fig. 5B) to check if there is additional defect which was not observed in the PMMA removal step or additional defects introduced during the pattern transfer. With optimized pattern transfer recipe, the missing hole defect per wafer of transferred via in the oxide is similar to the total PMMA removal level (5 ea defects/wafer) as shown Fig. 5C.

Fig. 5. DSA via shrink before and after pattern transfer. (A) After PMMA removal, (B) After oxide etch, (C) Defect counts before and after pattern transfer.

4. Conclusion

The main goal of this study is to identify the defect types, defect sources and investigate methods for defect reduction. The fall-on and residue defects can be reduced from 353 to 117 ea defects/wafer. For missing hole defects, applying best known method can significantly reduce the missing hole defects from 40 ea defect per wafer to single digit defect count per wafer. Finally, pattern transfer is optimized and the defect level of DSA vias in the oxide layer is similar to the defect level before pattern transfer. This indicates that the materials and process of single DSA via shrink can be tuned to low defect level for potential implementation.

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