Negative-tone Photodefinable Underfill Having High Resolution and Appropriate Thermal Fluidity

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Photodefinable wafer level underfill (PWLUF) has been evaluated for chip to substrate stacking. The good fluidity of PWLUF after patterning is required for chip and substrate stacking. PWLUF was designed using polyimide, acrylates, epoxides and some additives. It was difficult to improve the fluidity of patterned PWLUF keeping resolution by changing the composition ratio of acrylates and epoxides. On the other hand, PWLUF using the polyimide oligomer obtained by increasing end capping agent ratio improved the fluidity as well as the resolution. The chip to substrate stacks afford void-free bump soldering without underfill entrapment. We also successfully demonstrated the reflow soldering process using PWLUF.

Keywords: Underfill, Polyimide, High fluidity, Resolution, End capping agent

1. Introduction

Today's packaging technologies require high density connections among the different kinds of devices, especially between dynamic random-access memory (DRAM) and logic IC. For these interconnections, the 3D vertical integration of DRAM on logic IC or the side by side integration of 3D stacked DRAM and logic IC using silicon interposer with TSV (Through Silicon Via) have been studied. However, TSV technology faces some issues such as poor high-frequency properties and high fabrication cost. Organic interposer with high density wiring is one of the key solutions for the trend of electronic package development [1]. The bumps on interposer become narrower for higher density connections. Underfill materials are filled between organic/inorganic substrate and chip for stress relief and reinpressionment of bump soldering. The conventional capillary underfill is difficult to be applied to the package with fine pitch bumps because the capillary process after stacking is slow and damages the fragile low k. Pre-applied wafer level underfill, which is formed to the whole wafer by lamination or spin coating, has been investigated. During the bonding process, the

underfill material must flow not to be trapped between bump and pad. The underfill entrapment worsens the reliability of device by interfering the formation of intermetallic compound between bumps [2]. As the bump numbers increase and the pitch narrows furthermore, it will be more difficult to push out the underfill on the top of bumps. Photodefinable wafer level underfill (PWLUF) was developed and its design concept was verified, that is, the removal of underfill on the top of bumps enables the excellent quality of bump connection without underfill entrapments. It also can control the amount of overflowed underfill [3,4]. In this paper, we report the PWLUF fluidity improvement keeping the resolution and the assembly results for chip on substrate stacks.

2. Experimental

PWLUF varnish was prepared by mixing a polyimide, acrylates, photoradical initiator, epoxides, curing components and NMP. The varnish was coated on polyethylene terephthalate film with release layer and pre-baked at 80 °C for 20 min, then 120 °C for 20 min in an oven. PWLUF

films were laminated on wafer with bumps at 80 °C by vacuum laminator. The resin over the bumps was removed by exposure through mask and development using 2.38% tetramethyl ammonium hydroxide aqueous solution. Table 1 shows the designs of chip and substrate. The chip has 38 μm square bumps with 45 μm height and the substrate has 20 μm thick solder resist and 9 μm thick Cu line and pad. Figure 1 shows the cross-sectional image of chip and the overview of substrate.

Figure 2 shows the thermal compression bonding process and Fig. 3 shows the bonding profile. This profile is the same as chip on chip bonding, which was confirmed to give the bump soldering without voids and entrapment [5]. Figure 4 shows the schematic reflow soldering process. The chips were bonded on substrate at 150 °C for 7 s at 20 MPa pressure and the stacked sample passed through reflow oven as shown in Fig. 5 [5].

Table 1. Chip and substrate structure for assembly evaluation.

Chip	7.3 mm $\times$ 7.3 mm, 150 μm chip thickness 328 pins, Peripheral, SiO_2 surface
Bump	Cu pillar (20 μm thickness) + SnAg solder (20 μm thickness) 80 μm pitch
Substrate	0.4 mm substrate thickness, 9 μm Cu thickness L / S = 40 μm / 40 μm

Fig. 1. Cross-sectional image of bumps on chip (a) and overview of substrate (b) for assembly evaluation.

Fig. 2. Schematic thermal compression bonding process. PWLUF Patterning (a), alignment (b) and bonding (c).

Fig. 3. Temperature profile (a) and pressure profile (b) of thermal compression bonding.

Fig. 4. Schematic reflow soldering process. PWLUF Patterning (a), alignment bonding (b) and reflow soldering (c).

Fig. 5. Temperature profile of reflow oven after alignment bonding.

3. Results and discussion

3.1. Chip on substrate stacking trial

The bump soldering technique without underfill entrapment has been successfully demonstrated for chip on chip stacks using PWLUF [3,4]. We have evaluated Material A as

PWLUF for chip on substrate stacks. The bump tops on chip were completely exposed by patterning of PWLUF as shown in Fig. 6. The obtained chips were bonded on the substrates by the bonding profile in Fig. 3. However, the stacks had no electrical connections. The bump soldering, delamination and voids were observed by the cross-sectional image from scanning electron microscope (SEM) and scanning acoustic microscope (SAM) for failure analysis. Figure 7 shows that the solder on chip was deformed to chip edge side and did not reach pad on substrate. As shown in Fig. 8, many voids were observed in no bump area. We supposed that the non-uniform resin flow caused by rugged surface of substrate pushed out the solder and brought connection failure as shown in Fig. 9. The 150 °C melt viscosity of patterned Material A was 1,200 Pa·s. We assumed that the low viscosity of PWLUF after patterning provides better bump soldering and prevents the solder deformation.

Fig. 6. Bird's eye view of bumps with patterned PWLUF.

Fig. 7. Cross-sectional SEM of stacked sample using Material A.

Fig. 8. SAM inspection of stacked sample using Material A.

Fig. 9. Supposed schematic cross-section of solder deformation using Material A.

3.2. Fluidity improvement of patterned PWLUF while maintaining resolution

We investigated an influence of acrylate and epoxy amounts with respect to the PWLUF viscosity after patterning and the resolution as shown in Table 2. Material B including acrylates of 0.7 times as much amount as Material A shows poor resolution in spite of lower viscosity than Material A. Material C including the epoxides of 1.3 times as much as Material A shows comparable viscosity and poorer resolution than Material A. From these results, it is not effective way to control the amounts of acrylates and epoxides for the fluidity improvement of patterned PWLUF while maintaining resolution.

The polyimide (PI-1.0) for Material A is obtained by the polycondensation reaction of tetracarboxylic dianhydride, diamine having phenol moiety and amino phenol as end cap agent. The molar content of tetracarboxylic dianhydride is more than that of the diamine to prevent monomer existence after the reaction. The gel permeation chromatography (GPC) confirmed that PI-1.0 has no monomers. We have studied the influence of the polymer molecular weight on the resolution and fluidity after patterning. The polyimide molecular weight was adjusted by the ratio of amino phenol as shown in Fig. 10.

Table 3 shows the list of polyimides which have the same main chain structure and different molecular weight. The number average molecular weights (M_n) of PI-1.5, PI-1.0, PI-0.7 and PI-0.5 are 25,000, 15,000, 11,000 and 6,700, respectively. There were no monomers from GPC. The obtained M_n values are the almost same as calculated ones in Fig. 10. Table 4 shows the minimum development time and aspect ratio of 20 μ m thick Material A, D, E and F including the same compositions as Material A except polyimide. Material F with the low molecular weight polyimide afforded short development time and high resolution. We supposed that these results were caused by molecular weight polymer and more phenol moieties. Figure 11 shows the influence of polyimide molecular weight on patterned PWLUF fluidity. Material F with the low

Table 2. Influence of acrylate and epoxy amount on the viscosity at 150 °C after patterning and resolution.

Material	Material A	Material B	Material C
Acrylates ¹⁾	1	0.7	1
Epoxides ²⁾	1	1	1.3
Viscosity ³⁾	1,200 Pa·s	1000 Pa·s	1,300 Pa·s
Resolution ⁴⁾

¹⁾ Relative amount of acrylates to Material A. ²⁾ Relative amount of epoxides to Material A.

³⁾ Viscosity at 150 °C after patterning.

⁴⁾ 20 μm thickness. Adjusted patterning condition.

Fig. 10. Schematic polyimide design having different molecular weight.

molecular weight polyimide achieved the low viscosity after patterning as expected. Figure 12 summarizes the 150 °C viscosity after patterning and aspect ratio using different polyimide molecular weight. Material F using PI-0.5 improved fluidity (150 °C viscosity: 240 Pa·s) after patterning as well as resolution property (aspect ratio: 2.0).

Table 3. Composition ratio of different molecular weight Polyimide.

Polyimide	PI-1.5	PI-1.0	PI-0.7	PI-0.5
Tetracarboxylic dianhydride	15	10	7	5
Diamine with phenol	14	9	6	4
Amino phenol	2	2	2	2
Mn	25,000	15,000	11,000	6,700

Table 4. Minimum development time (M.D.) and aspect ratio using different molecular weight Polyimides.

Material (Polyimide)	Material D (PI-1.5)	Material A (PI-1.0)	Material E (PI-0.7)	Material F (PI-0.5)
M.D. ¹⁾ (s)	120	30	20	15
Aspect ratio ²⁾	0.5	1.3	1.3	2.0

¹⁾ 20 μm thickness.

²⁾ Same exposure dose. Development time is M.D. × 1.5.

Fig. 11. Influence of polyimide molecular weight on PWLUF viscosity after patterning.

Fig. 12. 150 °C viscosity after patterning and aspect ratio using PWLUF with different molecular weight polyimide.

3.3. Chip on substrate assembly evaluation

Material F was evaluated for the chip on substrate stacks using the same profile as shown in Fig. 3. Figure 13 shows the cross-sectional SEM image of bump and SAM of stacked sample by thermal compression bonding. Material F achieved 100% electrical yield and excellent bump soldering without any underfill entrapment between bumps and voids. Next, we have evaluated the compatibility of the patterned PWLUF with chip stack on substrate by reflow soldering after alignment bonding at 150 °C for 4s by 20 MPa pressure as shown in Fig. 3. The reflow soldering is the promising process to improve the productivity of pre-applied underfill. The stacked sample

Fig. 13. Cross-sectional SEM image of bump (a) and SAM image (b) of the chip stack on substrate obtained by thermal compression bonding using Material F.

Fig. 14. Cross-sectional SEM image of bump (a) and SAM image (b) of the chip stack on substrate obtained by reflow soldering process using Material F.

F afforded 100% electrical yield and excellent bump soldering with few voids from cross-sectional SEM and SAM inspection in Fig. 14. From these results, we have verified that PWLUF achieved chip stack on substrate by reflow soldering as well as thermal compression bonding.

4. Conclusion

We have developed PWLUF with high resolution and appropriate fluidity for the chip stack on substrate. The stacked sample using Material A had no electrical connection because of the high viscosity at 150 °C after patterning. It was difficult to satisfy both low viscosity and high resolution by changing the composition ratio of acrylates and epoxides. Material F using low molecular weight polyimide gave its viscosity at 150 °C after patterning low with improvement of aspect ratio of lithographic pattern. The chip stack on substrate using Material F afforded void-free bump soldering without underfill entrapment. The reflow soldering process was also successfully demonstrated to improve the productivity of pre-applied underfill.

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