The Status of Nanoimprint Lithography for High Volume Semiconductor Manufacturing

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Imprint lithography is an effective and well known technique for replication of nano-scale features. For the purpose of semiconductor device fabrication, nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. In this paper we describe the latest performance update of the equipment, and to discuss the alignment system and overlay methods needed to yield advanced semiconductor devices. Throughputs of up to 90 wafers per hour have been achieved using a cluster system approach. On tests wafers a mix and match overlay of 3.2 nm is demonstrated. Additionally, a Drop Pattern Compensation (DPC) method is introduced as an additional means for improving overlay. Finally, to address cost of ownership, a mask lifetime of over 300 wafer lots has been demonstrated.

Keywords: Nanoimprint lithography, NIL, Throughput, Overlay, Mask life, Drop pattern compensation

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features [1,2]. For the purpose of semiconductor device fabrication, nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate [3-9]. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

This paper introduces the latest performance update of the equipment. Specifically, we describe progress on throughput, overlay and mask life.

2. Throughput

Throughput is one of the key contributors to cost of ownership. In this section, we discuss how throughput was enhanced to 90 wafers per hour. Canon uses a multi-module approach to achieve high throughput. The NZ2C cluster tool typically is configured with four imprint modules or stations. Previous papers have discussed throughput breakdown in detail [10]. Overheads to the imprint TAKT time have been reduced by applying a multi-field dispense strategy, as opposed to dispensing and imprinting in a sequential fashion (see Fig. 1). The reduction in overhead is on the order of 0.24 seconds, resulting in an increase in throughput to 90 wafers per hour. Figure 2 shows that non-fill defectivity is nominally the same for the multi-field approach.

3. Alignment and overlay

The NZ2C system employs a Through The Mask
Fig. 1. By continuously dispensing, overhead times are reduced by 0.24 seconds per field, thereby enhancing throughput to 90 wafers per hour.

Fig. 2. Defect inspection result comparison. The multi-field dispense results are comparable in defectivity to the sequential imprinting method.

(TTM) alignment system. First order terms are passed through Moiré marks on the mask and wafer with a sensitivity on the order of 1 nm. On device wafers, it is possible to enhance the align signal and avoid blooming by using multiple wavelengths, and controlling the intensity of each wavelength. The method aids in controlling signal variations, resulting in reduced measurement errors.

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool in order to do high order distortion controls (HODC). HODC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Heat input on a field by field basis is realized through the use of DMD array which imparts heat through the mask onto a stepper field of a wafer. The basic operation of the system, along with initial results has been described in previous publications [11,12]. The system is shown schematically in Fig. 3.

Fig. 3. Schematic illustration of the HODC system used to correct in-field distortions.

The TTM and HODC systems were applied to test wafers and the results are reported in Figs. 4 and 5. Figure 4 depicts Cross Matched Machine Overlay (XMMO) on an existing level patterned with an ASML 1950 ArF immersion tool. A total of 84 fields were measured, including twelve points per field. The results are an average across 23 wafers. XMMO of 2.9 nm and 3.2 nm mean plus three sigma was achieved in x and y, respectively.

Fig. 4. Cross matched machine overlay of 3.2 nm, 3 sigma has been demonstrated on test wafers.
Similarly, Figure 5 depicts Single Machine Overlay on an existing level patterned with the FPA-1200 NZ2C tool. A total of 84 fields were measured, including twelve points per field. The results are an average across three wafers. SMO of 2.2 nm and 2.4 nm mean plus three sigma was achieved in x and y, respectively. Residual distortions were 0.7 nm, mean plus three sigma.

In addition to the Magnification actuator that is used to correct linear terms and the HODC system that is used to correct higher order terms, a third “knob” is also available for field by field distortion correction. In a typical nanoimprint process, resist is dispensed to fill all relief images on the mask and create a uniform residual layer beneath the patterned features. Drop Pattern Compensation (DPC) is used to create a drop pattern to match non-flatness and other induced distortions and minimize overlay errors. This means that DPC can be used to address lithography related errors including:

1. Chuck induced errors
2. Pattern induced distortions
3. Grid distortion errors from an optical scanner
4. Stress induced distortion from previous levels.

In addition, for nanoimprint lithography, DPC can address mask bending induced overlay errors. A schematic illustration of the DPC process is shown in Fig. 6.

A DPC example is shown in Figs. 7, 8a and 8b. The figure below depicts the topography on a device-like wafer in which the areas between the die within the field are recessed by about 20 nm.

In addition, for nanoimprint lithography, DPC can address mask bending induced overlay errors. A schematic illustration of the DPC process is shown in Fig. 6.

Fig. 5. Single machine overlay of 2.4 nm has also been demonstrated on test wafers.

Fig. 6. Using DPC, the resist film thickness is optimized to match mask and wafer bending.

Fig. 7. The topography on a device-like wafer, in which the areas between the die within the field are recessed by about 20 nm.
The topography induces overlay errors when patterning on top of this layer as shown in Fig. 8a. The 3 sigma errors are on the order of 5.4 nm, and the effect of the recessed areas within the field are easily observed. By applying both HODC and DPC, the overlay errors are reduced to 3.4 nm, 3σ, and the impact of the recesses are clearly reduced.

Fig. 8. Overlay is impacted by the 20 nm recessed topography on a device-like wafer. By applying both HODC and Drop Pattern Compensation (DPC), the overlay errors are reduced from 4.4 nm in x (a) to 3.4 nm in x and 3.3 nm in y (b).

4. Mask life

NIL requires both a master mask and multiple copies of a replica mask. As a result, the gating item on cost for NIL the mask life of the replica mask. In 2017 the mask life target of 80 wafer lots was met. This year, Toshiba Memory Corporation has demonstrated a mask life of over 300 lots (Fig. 9) [13]. The increase in mask life has been driven by a variety techniques designed to mitigate particles in the wafer tool. The techniques cover source control, particle avoidance and particle collection, as shown in Fig. 9. As a next step, we are considering the implementation of on-tool mask cleaning.

Fig. 9. Mask life history. This year, Toshiba Memory Corporation has a demonstrated a mask life of over 300 lots.

5. Conclusion

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay, throughput and defectivity. In previous papers, overlay and throughput results have been reported on test wafers. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results on both test wafers and device wafers. On test wafers, XMMO of 2.9 nm and 3.2 nm in x and y respectively was demonstrated. SMO of 2.2 nm and 2.4 nm was achieved, with an opportunity to further improve results by applying wafer chucks with better flatness specifications. Additionally, a new method for reducing overlay errors, Drop Pattern Compensation (DPC) was introduced, and an example was presented showing the how DPC could be used to overcome existing pattern topography on a wafer. Finally, defectivity has been addressed by reducing particles generated in the imprint tool, thereby extending mask life to more than 300 wafer lots. Mask life extension is an important factor in improving NIL cost of ownership.

Acknowledgments

The authors gratefully acknowledge the support of their colleagues at both Canon Inc. and Canon Nanotechnologies, Inc. Further, the authors would like to thank both DNP and TMC for their efforts in
advancing nanoimprint lithography.

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