Multi-Level Nanoimprint Lithography for Large-Area Thin Film Transistor Backplane Manufacturing

Tamer Dogan^{1,2}, Joris de Riet¹, Thijs Bel¹, Roy Verbeek¹, Ilias Katsouras¹,
Eric Meulenkamp¹, Gerwin Gelinck^{1,2}, and Auke Jisk Kronemeijer^{1*}

¹ TNO / Holst Centre, High Tech Campus 31, NL-5656 AE, Eindhoven, The Netherlands

² Department of Applied Physics, Eindhoven University of Technology,
5600MB, Eindhoven, The Netherlands

*auke.kronemeijer@tno.nl

Thin film transistors (TFTs) are the basis for current AMOLED display arrays. For next-generation displays, higher resolution and cost-effective manufacturing of panels is adamant. The current benchmark patterning method in the display industry is photolithography. Here, we propose the use of a hybrid approach of nanoimprint lithography and conventional FPD processing for the realization of high-resolution display backplanes. We demonstrate the realization of sub-micron amorphous oxide semiconductor TFTs with multi-level nanoimprint lithography in order to decrease the number of patterning steps in display manufacturing. Top-gate self-aligned a-IGZO TFTs are realized with performance comparable to benchmark photolithography-based TFTs.

Keywords: a-IGZO TFT, multi-level nanoimprint lithography, AMOLED

1. Introduction

The display industry continues to increase display quality, expressed in performance metrics such as e.g. higher resolution, higher brightness, better color gamut, increased contrast and decreased power consumption. Equally, the cost of manufacturing of displays has been actively decreased with the industry searching for cost-effective, large-area processing technology.

For AMOLED displays, resolution is determined by the underlying large-area patterning capabilities of TFT backplanes by photolithography, as well as display front planes by e.g. fine metal mesh evaporation masks. For the realization of the TFT backplane, the industry is searching for cost-effective, high resolution patterning techniques with a high throughput. The current benchmark for patterning is subtractive photolithography implemented in large-area tools.

Nanoimprint lithography (NIL) is a patterning technique that is able to realize high-resolution patterns at low cost [1,2]. It is a contact-based process which involves pressing a template mold into a soft deformable resist material. The mold can be rigid, soft, flat or a drum depending on

technology implementation chosen for either sheet-to-sheet or roll-to-roll processing. Various reports have described the realization of TFTs, with various semiconductor channel materials, using nanoimprint lithography [3-7]. A notable example is the developed Self-Aligned Imprint Lithography (SAIL) process by HP, where TFT manufacturing has been demonstrated by roll-to-roll realization of (metal oxide) TFTs with micrometer channel lengths [8,9].

Substrate conformal imprint lithography (SCIL) is a specific implementation of imprint lithography with advantages of both rigid and soft molds. SCIL has been used to pattern 3D photonic structures, nanowire growth templates and other structures in photovoltaic and photonic applications [10-13].

Here we realize TFTs with a hybrid nanoimprint lithography approach for use in high-resolution AMOLED displays. The hybrid approach, compared to SAIL, is chosen in order to overcome pixel design limitations for AMOLED driving. We demonstrate the realization of sub-micron a-IGZO TFTs using multi-level nanoimprint lithography with performance comparable to benchmark photolithography-based TFTs.

Fig. 1. Basic pixel schematics for LCD and OLED displays.

2. AMOLED pixel designs & imprint lithography

OLED light emission is a current-driven technology as compared to the LCD implementation where backlight transmission is modulated by voltage-driven switching of LC materials. This difference has implications for the structure of the most simple switching element, i.e. pixel, used in display array. The simplest variant for an LCD display consists of single transistor to switch the voltage on a pixel electrode to which the LC material will adapt because of a changing electric field over the material. In contrast, the simplest OLED pixel structure consists of two transistors and a capacitor (see Fig. 1). The switch (select) transistor is used to charge the gate of the second (drive) transistor to an extent that a prescribed amount of current is driven by this transistor through the OLED frontplane to result in the desired light output. The capacitor is used in the pixel to keep the desired charged stated of the drive transistor constant within the refresh period of the full display array.

The need for the use of a different pixel engine for AMOLED display driving has implications for the TFT technology implementation that can be used for the realization of the backplanes. Crucially, as can be observed from Fig. 1, the AMOLED pixel engine technology needs to be able to realize an electrical connection between the source-drain contact of the select transistor with the gate of the drive transistor. For monolithic realization of AMOLED displays, this means the need for a via interconnection between the TFT technology source-drain metallization layer and the gate metallization layer. The full SAIL TFT process, by virtue of the deposition of all relevant TFT material layer before patterning by imprint lithography, is not

capable of realizing these interconnects in a monolithic manufacturing process. To this end, we developed a hybrid TFT process, that benefits from the use of nanoimprint lithography for the realization of high patterning resolution, combined with subsequent lithography steps as in conventional FPD processing in order to realize the needed via interconnection between metallization layers.

In the hybrid development approach, the promise of using multi-level nanoimprint lithography to simplify the TFT manufacturing process remains, by encoding information of multiple layers in a single imprint step. Added value of this approach is a possible cost-reduction by reduction of the number of lithography mask steps, as well as improved resolution by realizing improved overlay accuracy between layers patterned in the same nanoimprint lithography cycle.

3. Multi-level nanoimprint for TFTs

Previously, we have reported on our benchmark self-aligned top-gate a-IGZO TFT process, both based on conventional photolithography for the patterning of relevant layers, as well as using single-level nanoimprint lithography for the realization of the gate stack in the TFTs [14,15]. The device architecture of these TFTs is shown in Fig. 2. Using single-layer nanoimprint, we demonstrated TFTs with channel lengths down to 450 nm with a field-effect mobility of 10 cm²/Vs and turn-on voltage close to 0 V [15].

The self-aligned top-gate architecture is beneficial from TFT performance point of view (parasitic capacitances, decoupling of gate dielectric and intermetal dielectric realization), as well as its compatibility with multi-level nanoimprint lithography manufacturing.

Fig. 2. Cross-section of self-aligned, top-gate a-IGZO TFTs.

Fig. 3. Schematic 3-mask step hybrid process flow for the realization of a-IGZO top-gate self-aligned TFTs.

Based on the single-level nanoimprint baseline process, we further developed the manufacturing process to implement multi-level imprint lithography to save a lithography mask step. Figure 3 demonstrates the schematic process flow developed, where the self-aligned TFT gate stack is realized with nanoimprint, and subsequently two photolithography steps are employed to pattern the intermetal dielectric and source-drain metallization layers. Details of the exact realization of the TFTs and process development will be described elsewhere [16].

In short, a buffer layer, a-IGZO, gate dielectric and metal gate are subsequently deposited by PECVD and room-temperature sputtering on a glass substrate. Next, imprint resist is coated on the layer stack and a 3D TFT structure for the top-gate stack and the a-IGZO semiconductor island (Fig. 4) is imprinted in the resist. Subsequent iterative wet- and dry-etching of imprint resist (residual layer)

Fig. 4. Master of the 3D structure of the self-aligned top-gate TFT structure encoding information for the a-IGZO semiconductor island and top-gate stack.

Fig. 5. Microscope image of fabricated self-aligned top-gate a-IGZO TFT realized by the hybrid multi-level nanoimprint process flow.

and TFT device materials (a-IGZO, gate dielectric and gate metal) result in the definition of the semiconductor island and TFT gate stack on top of the island. The TFT is finished by deposition of a PECVD intermetal dielectric and source-drain metallization, patterned by conventional photolithography. The ability to separately pattern these layers compared to the other layers in the TFT stack results in the specific capability to realize electrical interconnects between the gate

metallization layer and the source-drain metallization layer. Figure 5 shows a realized a-IGZO top-gate self-aligned TFT ($W/L = 10/4$) fabricated using the hybrid multi-level nanoimprint process flow.

4. TFT Performance

Figure 6 shows the transfer characteristics as a function of device channel length, demonstrating functional TFTs down to $0.7\ \mu\text{m}$. Extracted mobilities are in the range of $10\ \text{cm}^2/\text{Vs}$ with turn-on voltages close to 0V , which is comparable to our previously described photolithography-based and single-level nanoimprint benchmark processes [14, 15].

Fig. 6. Transfer characteristics of a-IGZO top-gate self-aligned TFTs fabricated by multi-level nanoimprint TFT process flow with channel length $L = 3.9, 3.0, 2.1, 1.2$ down to $0.7\ \mu\text{m}$.

5. Conclusion

We have realized functional top-gate self-aligned a-IGZO TFTs with a hybrid multi-level nanoimprint lithography approach to decrease the number of patterning steps in AMOLED backplane manufacturing. The hybrid approach is used to enable AMOLED pixel schemes that require the electrical interconnection between gate and source-drain metallization layers – something the full SAIL process cannot monolithically attain. TFT performance is comparable to benchmark photolithography-based TFTs. The results demonstrate the feasibility of the use of multi-level nanoimprint lithography in a hybrid FPD process flow to cost-effectively realize high resolution TFT backplanes.

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