Advances in X-ray Lithography at ASET

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In ASET, in cooperation with NTT, we have developed key systems for X-ray lithography (XRL) such as X-ray steppers and a 100-kV electron-beam (EB) lithography system for x-ray mask fabrication. Mask-to-mask overlay accuracy within 20 nm (3σ) between the gate- and contact-hole-layers for 1-Gb DRAM has been achieved. Critical dimension (CD) control of ± 14 nm for the gate and ± 10 nm for the contact-hole-patterns have also been realized. The advantages of XRL over advanced optical lithography, in terms of both resolution and process latitude, were demonstrated through computer simulation. The outcomes of several experiments have convinced us that XRL is a particularly promising technology for mass-producing 0.1- μm or smaller devices.

Keywords: X-ray lithography, X-ray stepper, X-ray mask

1. Introduction

ULSIs with minimum feature sizes as small as 0.10 μm to enable dense patterns are expected to be mass-produced by 2005. To achieve this with optical lithography, various complicated technologies, such as phase-shift masks, optical proximity correction, anti-reflection coatings, and planarization will be required. These technologies will make the lithography cost extremely expensive. In addition, future optical lithography systems themselves will be much more expensive than conventional one. As a result, the lithography cost might raise the device cost even though devices are down-sized. For us to continue benefiting from device miniaturization, a form of cost-effective next-generation lithography (NGL) needs to be developed.

X-ray lithography (XRL) offers high resolution, a large process margin, and cost effectiveness. To apply XRL to 0.10- μm device processes, however, high-precision systems and masks will have to be developed. In ASET, we have been developing core systems for XRL, such as X-ray steppers and a high-precision 100-kV EB writer in cooperation with NTT. Using these tools, we have developed XRL processes, and have applied them to device fabrication so that we could assess this family of technologies in practical use.

Through these activities, we are convinced that XRL can be applied to 0.10- μm or smaller device production.

In this article, we describe the recent progress of XRL technology at ASET and examine the remaining issues that need to be resolved to allow the practical implementation of XRL.

2. Key-systems developed at ASET

During the last four years, we have developed several key systems for applying XRL to sub-0.1- μm device fabrication. In 1997, we installed an X-ray stepper, the XS-1 (Fig. 1)[1], which was developed based on NTT's technologies. We have since used the XS-1 stepper in mask-alignment tests for various kinds of processed wafers, and in the replication of extremely fine patterns (down to 60-nm line-and-space patterns) for an extendibility study.

To enable a practical throughput as high as 60 wafers/h, a new X-ray stepper XRA was developed by Canon, and was installed at ASET's Amagasaki branch in Dec. 1999. The XRA is capable of magnification correction[2], which reduces overlay error caused by process-induced systematic wafer distortion. The XRA has been tuned and is expected to be in full operation in April, 2000.

In addition, the EB-X3 (Fig. 2) [3], which was developed by NTT in cooperation with ASET, is the first system specifically designed for X-ray mask fabrication. The principal specifications of the EB-X3 and its current capabilities are listed in Table 1.

Fig. 1 The prototype X-ray stepper; XS-1 installed in a thermal chamber with a chemical filter.

Fig. 2 100-kV EB lithography system (EB-X3) developed for X-ray mask fabrication.

Table 1 Specifications and current capabilities of the EB-X3.

Item	Spec	Current
Beam acceleration voltage	100 kV	←
Beam current density	50 A/cm ²	←
Beam edge resolution	25 nm	←
Address unit	1 nm	←
Resolution	50 nm	←
Image placement accuracy	≤ 10 nm	≤ 15 nm

3. X-ray mask

Critical dimension (CD) control and image-placement accuracy in high-density mask delineation with the EB-X3 has been evaluated with 1-Gb DRAM patterns (Fig. 3). The patterns used to measure overlay-error and CD-control were placed among the memory-cell patterns of a 1-Gb DRAM. The X-ray masks for gate-layer and contact-hole-layers were fabricated at NTT and NTT-AT. The mask pattern was delineated with a multi-path (four steps) writing scheme[4] in a 0.2- μ m-thick positive resist (ZEP-520). The CD error was measured with an SEM linewidth-measurement system.

Fig.3 Pattern layout of a mask for measurement of CD-control and overlay-error. Memory-cell patterns for a 1-Gb-DRAM are arrayed in the gray area.

Figure 4 shows the CD error in resist-pattern formation for the gate- and contact-hole-layer masks. CD-error smaller than 19 nm (gate) and 10 nm (contact-hole) has been achieved in both masks.

Image placement accuracy of resist-pattern on the masks was measured using a laser-interferometric coordinate measurement system (Leica LMS-I PRO). The best image placement data in EB writing from the masks for the gate-layer of a 1-Gb DRAM is shown in Fig. 5. Both the maximum error and the 3σ value were smaller than 10 nm. Thus, this mask provided the image placement accuracy required for masks used in 0.1- μ m ULSI device fabrication.

Fig. 4 CD control in resist patterning with EB-X3 for the gate- and contact-hole-patterns of 1-Gb-DRAM masks.

Fig. 5 The best image placement accuracy of EB-resist pattern in the gate-layer mask for a 1-Gb DRAM.

Wiring patterns with a minimum feature size of 85-nm and 80-nm-diameter contact-hole patterns were formed in a ZEP-520 resist using EB-X3 without any proximity-effect correction (Fig. 6)[3].

These experimental results have convinced us that X-ray mask pattern delineation is no longer the limiting factor in X-ray mask fabrication.

Fig.6 Wiring pattern with a 85-nm minimum feature size (left) and an 80-nm-diameter hole pattern (right) delineated with the EB-X3 in a 0.2- μ m-thick positive resist (ZEP520).

4. Applicability in practical wafer-processes

4.1 Overlay accuracy and CD control

In practical device-fabrication processes, mask-alignment will be done for wafers under various conditions. We have carried out a variety of experiments using the XS-1 to evaluate the mask-to-mask overlay accuracy and CD control on processed wafers in co-operation with NTT and member companies of the ASET XRL group. Table 2 lists the main experiments. Here, we will briefly review some of these experiments.

Table 2 Experiments carried out at ASET in collaboration with member-companies to prove usefulness of XRL in practical processes.

Company	Theme of experiments
Fujitsu	Sub-100-nm transistor fabrication applying XRL at five layers
Hitachi	Comparison with advanced optical lithography by simulation
Mitsubishi	64-Mb DRAM processes applied with XRL at two layers
NEC	Evaluation of CD control and overlay accuracy at gate and contact-hole layers for 1-Gb DRAM
Toshiba	Alignment test for wafers after CMP process

ASET and NEC have quantitatively analyzed the overlay-error between the gate- and contact-hole layers for 1-Gb DRAM and the CD control at each process. The X-ray masks for these experiments were supplied by NTT-AT. The masks were made of 2- μm -thick diamond membranes on which 0.35- μm -thick α -Ta X-ray absorber patterns were fabricated. The diamond membrane was stretched over a 2-mm-thick Si frame, that was supported by a 5.6-mm-thick, 5-inch-square Pyrex-glass frame (Fig.7).

Fig. 7 X-ray mask used to pattern the gate-layer for a 1-Gb DRAM.

The magnification error arising from wafer processes was corrected by controlling the wafer temperature during the X-ray exposure[6]. The wafer temperature was controlled to reach an appropriate value on the wafer-rotation-match unit. The magnification correction was kept throughout the X-ray exposure by holding the wafer on the wafer stage by vacuum-chucking.

A photograph of a wafer after contact-hole-pattern replication is shown in Fig. 8. The entire area was exposed with 37 shots by step-and-repeat printing.

The total overlay error (mean + 3σ) between the gate- and contact-layer for 12 wafers was measured using an overlay measurement system (KLA-5100), and was within 47 nm. The best data was less than 40 nm as shown in Fig. 9.

CD-control data for gate- and contact-hole-patterns replicated into resist films has been taken from 2960 points on five-wafers for each pattern (Fig. 10). The targeted size were 130 nm for both the gate and contact hole. Mean(offset) + 3σ for gate- and contact-hole-patterns were 16.1 nm and

Fig. 8 8-inch-diameter wafer exposed with 37 shots for contact-hole layer of 1-Gb DRAMs by step-and-repeat printing.

Fig. 9 Total overlay error between the gate- and contact-hole-layers for 1-Gb DRAM processes in the best sample.

8.2 nm, respectively. The principal factors for the CD-error were pattern width error in the X-ray masks and X-ray intensity distribution in the exposure field. There is a room for further improvements in both of these error-factors.

4.2 Comparison with optical lithography

ASET and Hitachi have simulated the pattern fidelity for a 0.1- μm minimum feature size with XRL as well as with ArF- and F₂-excimer laser lithography using Levenson-type phase-shift

Fig. 10 CD control for gate and contact-hole patterns for 1-Gb DRAMs.

masks[7]. The mask-to-wafer proximity gap for XRL was 10 μm . The optical stepper's numerical aperture was 0.68 for ArF and 0.75 for F_2 . Figure 11 shows one of the simulated model patterns with a 0.1- μm minimum feature size.

Fig.11 A simulated model pattern with 0.1- μm minimum features.

Simulated aerial images and a resist pattern replicated in ZEP-520 resist by XRL are shown in Fig. 12. XRL clearly offers good fidelity, whereas the pattern profiles with ArF and F_2 are seriously degraded; also, the focus-margin is less than 0.2- μm , even in the case of F_2 .

5. Future plans

In FY2000, we are planning to achieve layer-to-layer overlay accuracy within 35 nm by using X-ray masks with high-density patterns with a 0.1- μm design-rule. By using these masks, we also expect to demonstrate CD control within ± 10 nm on processed wafers. Achieving a

Fig.12 Simulated aerial image profiles for the pattern shown in Fig. 10. Only XRL showed a good profile in both the simulated and actual resist patterns.

throughput of more than 60 wafers/h is another important goal. Most of the planned experiments will be done in collaboration with NTT and ASET's member companies with a new X-ray stepper, the XRA.

6. Summary

We have met our target specifications for a newly developed EB lithography system (the EB-X3) in collaboration with NTT. Using both a multi-path-writing scheme and PAT method, we have also realized image-placement-accuracy and CD control of within 10 nm in a gate-layer mask for 1-Gb DRAMs. A wiring pattern with an 85-nm minimum feature size and a 80-nm hole pattern were well defined in a 0.2- μm -thick positive resist without any proximity-effect correction. These results demonstrate the usefulness of the EB-X3 for fabricating X-ray masks with a 0.1- μm design-rule.

The total overlay error between the gate- and

contact-layers for 1-Gb DRAMs (which included the mask-distortion, wafer-distortion, mask alignment error, and measurement error) was within 47 nm (3σ) for 12 wafers. CD control in the resist pattern for the gate- and contact-layers was 16.1 nm and 8.8 nm (offset + 3σ), respectively. Further improvements in both overlay accuracy and CD control, and the demonstration of higher throughput, will be achieved in FY2000.

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