Implementation of ArF Resist Processes for 130nm and below

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About one year ago, first generation full field ArF step and scan systems (193nm) have been introduced and this has triggered a lot of activity in 193 nm lithography. Significant progress has been made in both ArF resist performance and exposure tool characterization. For introduction of 193 nm technology, a lot will depend on the maturity of the 193nm resists. Besides lithographic performance, dry etch selectivity with respect to various substrates will play an important role as well as other integration aspects such as BARC compatibility and proximity effects. In this paper, the status of ArF lithography is reviewed for the 130nm node with emphasis on the integration aspects. It will be demonstrated that the state-of-the-art 193nm resists can already be used for integration in critical layers (gate and contacts) of typical CMOS processes. Initial results for the 100nm node using alternating phase shifting masks and quadrupole illumination look very promising for 193nm.

Keywords : ArF lithography, 130nm node, 193 nm resists, resolution enhancement

1. Introduction

Following the latest issue of the ITRS roadmap, the 130nm node will be inserted in volume manufacturing in 2002, and the most aggressive companies claim that they will start already in 2001. Lithographers are preparing their processes for the 130nm node. Basically two options exist: inserting 193nm technology or pushing 248nm to its limits. About one year ago, first generation full field ArF step and scan systems (193nm) have been introduced in a number of fabs. These systems have lenses with numerical apertures (NA) in the order of 0.6. At the same time, 0.7 NA KrF step and scan systems (248nm) have been introduced as well. 193nm lithography is a new technology that needs a lot of further development. However significant progress has been made in both ArF resist performance and exposure tool characterization [1-4]. The first generation ArF step and scan systems are designed for R&D and pilot line operation rather than volume production. The first ArF projection lenses have NA's that go up to approximately 0.6 and CaF$_2$ is used in the critical points along the optical path. 193nm volume production is foreseen on the second generation step and scan systems, which will have higher NA lenses (≥ 0.70 NA) and higher throughput.

The first impression of the resolution capability of a lithography process can be obtained from the Raleigh equation. As can be seen in table 1, the $k_1$ factor corresponding to 130nm features printed on a 0.63 NA ArF scanner is exactly the same as the $k_1$-factor for 130nm when printed on a 0.8 NA KrF system: 0.42. 0.8 NA KrF step and scan systems are being developed by most major stepper manufacturers but are not yet available. The highest NA available today on a KrF step and scan system is 0.7. On such a system, the $k_1$ factor is significantly lower: 0.37. However, given the lower maturity of 193nm resists it is not unexpected that 248nm lithography will allow lower $k_1$ factors in KrF lithography.

From this table, it also becomes clear that 193nm should be extendible down to the 100nm node with the availability of higher NA scanners (0.7 to
and when it will have reached $k_1$ factors of 0.36.

\[
\begin{array}{cccccc}
\lambda [\text{nm}] & 248 & 248 & 193 & 193 & 193 \\
 & 0.63 & 0.7 & 0.8 & 0.63 & 0.7 & 0.8 \\
150 & 0.38 & 0.42 & 0.48 & 0.49 & 0.54 & 0.62 \\
140 & 0.36 & 0.40 & 0.45 & 0.46 & 0.51 & 0.58 \\
130 & 0.33 & 0.37 & 0.42 & 0.42 & 0.47 & 0.54 \\
120 & 0.30 & 0.34 & 0.39 & 0.39 & 0.44 & 0.50 \\
110 & 0.28 & 0.31 & 0.35 & 0.36 & 0.40 & 0.46 \\
100 & 0.25 & 0.28 & 0.32 & 0.33 & 0.36 & 0.41 \\
90 & 0.23 & 0.25 & 0.29 & 0.29 & 0.33 & 0.37 \\
80 & 0.20 & 0.23 & 0.26 & 0.26 & 0.29 & 0.33 \\
70 & 0.18 & 0.20 & 0.23 & 0.23 & 0.25 & 0.29 \\
\end{array}
\]

Table 1: $k_1$ factors.

In this work, the status of 193nm lithography for the 130nm node is reviewed with emphasis on the resist process performance and integration issues. Some preliminary data are shown illustrating the performance of 193nm lithography for the 100nm technology node.

2. Experimental conditions

The 193nm exposures have been carried out on an ASML-PAS5500/900 ArF step&scan system, equipped with a 0.63NA projection lens (Carl Zeiss) and a Novaline-Litho193-07 ArF laser (Lambda Physik). In the IMEC pilot line, the step and scan system is interfaced to an ACT8 coat and development track (Tokyo Electron Ltd.). The litho cluster is fully charcoal filtered and the ammonia levels are continuously recorded using a Total Molecular Base Real Time Monitoring system (Extraction Systems Inc.). The ammonia levels measured in the lithography tools were below 1 ppb.

All experiments were carried out using the most advanced 193nm single layer and bi-layer photoresists. For line/space applications a resist thickness of 400nm has been used while for contact hole applications the resist was 500nm thick. The resists were coated on top of an optimized anti-reflective coating (organic or SiON). The resist materials were processed according to the conditions (soft-bake and PEB bake) as recommended by the suppliers. In case of the bi-layer resist, the TIS2000 process (ARCH chemicals) consisted of a 265 nm thick imaging layer on top of 400nm organic bottom layer.

The CD measurements were carried out using a KL8100-ER top-down scanning electron microscope (SEM). Cross-sectional micrographs were made using a Philips XL30 SEM. Data analysis was done using ProData (v. 2.0) and Klarity CD.

For the bi-layer resist [5], dry development [6-8] of the bottom layer was carried out in a LAM alliance TCP9400SE reactor using an O₂/SO₂ chemistry.

Etching of a 150nm P-doped Polysilicon layer has been carried out in a LAM TCP9400 PTX reactor using a three step process (breakthrough etch, main etch and overetch). The main etching step was based on a HBr/Cl₂ chemistry.

Oxide etching was carried out in a LAM 4520XL using a C₁₃F₈ chemistry.

3. 193nm imaging performance

For introduction of 193 nm technology, a lot will depend on the maturity of the 193nm resists. Besides lithographic performance dry etch selectivity with respect to various substrate will play an important role as well as other integration aspects such as BARC compatibility, proximity effects, mask error factor (MEF) in the selection process [9-10]. The lithographic performance of advanced single layer resists is demonstrated in section 3.1 and the effect of the illumination conditions on process windows and proximity effect is described in section 3.2.

3.1 Resist performance

A screening has been carried out of resist materials from different supplier. The basic lithographic performance of the resists has been tested including: resolution, linearity, processing windows, proximity, delay stability, line edge roughness, etch resistance. The compatibility of the resists with inorganic (SiON) and organic ARCs has also been considered.

If we compare the current status of the 193 nm resist with the performance of the resist one year ago, we see a steadily improvement. A good compatibility of the resists is seen with both organic and inorganic BARC materials. Dedicated resist materials are becoming available for L/S applications, isolated line applications and contact holes.
A large number of resists have been screened for implementation on the gate level for logic design rules. A resist for the gate level was evaluated for 130nm lines at a minimum pitch of 330nm up to fully isolated lines. Conventional illumination setting using a NA=0.63 and a partial coherence of 0.65 has been used for the resist screening. Although we do look at the performance on both organic and inorganic ARC, emphasis for this evaluation has been put on SiON as ARC material. The substrate used for the evaluation was a 24 nm SiON layer on top of a 150nm Polysilicon layer. The compatibility of several resists with the SiON is illustrated in Fig. 1.

![Profiles of 130nm isolated line and 130nm semi-dense lines (130nmL/200nmS) in different resist materials on SiON substrates.](image)

**Fig. 1:** Profiles of 130nm isolated line and 130nm semi-dense lines (130nmL/200nmS) in different resist materials on SiON substrates.

Sumitomo PAR710 is a resist developed for line/space applications while the other material (resist A, resist Z and JSR AT 111 S) are dedicated semi-dense to isolated line resists. All four resists show a good compatibility with the SiON substrate, as no or very limited footing is observed. In terms of profiles PAR710 and AT111S are the better performers. The higher optical absorption of Resist A resulted in sloped profiles. Resist Z shows excellent profile control for the isolated line but the semi-dense lines already have a deteriorated profile. JSR AT111S and Sumitomo PAR710 have been evaluated into more detail. The sensitivities of the resists are in the range of 6 to 8 mJ/cm². A linear resolution for the isolated lines of 100nm and 110nm was found respectively for the AT111S (Fig. 2) and for the PAR710.

The profiles of 130nm semi-dense (130nm L/200nmS) and isolated line through focus are illustrated in Fig. 3 and 4 for both resists.

![130nm lines (isolated and 1:1.5 line/space ratio) through focus for Sumitomo PAR710.](image)

**Fig. 3:** 130nm lines (isolated and 1:1.5 line/space ratio) through focus for Sumitomo PAR710.

![130nm lines (isolated and 1:1.5 line/space ratio) through focus for JSR AT111S.](image)

**Fig. 4:** 130nm lines (isolated and 1:1.5 line/space ratio) through focus for JSR AT111S.

Exposure-Defocus (ED) windows for 130nm iso and semi-dense lines have been measured top/down on a KLA8100ER system as illustrated in Fig. 5 and 6. For both resists a large overlap is seen for the 1:1.5 and isolated 130nm ED-window. By fitting a rectangle in the ED-window, the Exposure latitude over a 0.4 µm focus range and the DOF at 8% exposure latitude have been calculated. These values are listed in table 2 for individual feature sizes as well as for the overlapping process windows. From this table it can be concluded that the latitudes of the JSRAT111S are larger than the ones for the Sumitomo PAR710.
In Fig. 7 the CD is plotted as a function of line/space ratio for 130nm features. As exposure dose, the energy was used to print the 130nm isolated line on target. When the isolated line is on target, the denser lines print at a larger CD. This iso-dense bias is resist dependent. The Sumitomo resist is a dense line resist. The iso-dense bias, meaning difference in line width between fully dense (1:1) and isolated 130nm line amounts up to 20nm. For the JSR resist, which is designed for semi-dense to isolated line patterning, it is not possible to open the 1:1 lines/spaces at the optimum dose to print the isolated line. However when considering only the pitches of interest for the logic design rules (1:1.5 up to isolated), both resists show acceptable proximity effect.

A critical issue with many 193 nm resist is PEB sensitivity. Target values should be < 3nm/°C. However for the materials tested here, values of 10nm/°C and 20nm/°C have been measured (Table 3). These high values of PEB sensitivity might have a significant effect on CD control and overall process integration. Therefore, the CD uniformity over the wafer has been measured on a 130nm isolated line. Despite the high PEB sensitivity, still reasonable values of CD uniformity are obtained. A total range (maximum-minimum CD) of 10nm and 15nm have been found respectively for PAR710 and JSR AT111S (table 3).

Table 2: Processing latitudes on SiON.

<table>
<thead>
<tr>
<th></th>
<th>PAR710</th>
<th>AT111S</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 nm iso</td>
<td>EL @ 0.4 um DOF</td>
<td>7.60%</td>
</tr>
<tr>
<td></td>
<td>DOF @ 8% EL</td>
<td>0.39 um</td>
</tr>
<tr>
<td></td>
<td>Best Energy</td>
<td>8 mJ/cm²</td>
</tr>
<tr>
<td>130 nm 1:1.5 L/S</td>
<td>EL @ 0.4 um DOF</td>
<td>12%</td>
</tr>
<tr>
<td></td>
<td>DOF @ 8% EL</td>
<td>0.63 um</td>
</tr>
<tr>
<td></td>
<td>Best Energy</td>
<td>7.7 mJ/cm²</td>
</tr>
<tr>
<td>overlapping latitudes</td>
<td>EL @ 0.4 um DOF</td>
<td>6.20%</td>
</tr>
<tr>
<td></td>
<td>DOF @ 8% EL</td>
<td>0.34 um</td>
</tr>
</tbody>
</table>

Table 3: PEB sensitivity and CD uniformity

Coat/exposure and Post-exposure delay (PED) delay test were carried out in filtered environment (<1 ppb ammonia). Both single layer resists were found to be very stable showing less than 5 nm line width change for post-exposure delays up to 45 minutes.

A critical issue with many 193 nm resist is PEB sensitivity. Target values should be < 3nm/°C. However for the materials tested here, values of 10 nm/°C and 20 nm/°C have been measured (Table 3). These high values of PEB sensitivity might have a significant effect on CD control and overall process integration. Therefore, the CD uniformity over the wafer has been measured on a 130nm isolated line. Despite the high PEB sensitivity, still reasonable values of CD uniformity are obtained. A total range (maximum-minimum CD) of 10nm and 15nm have been found respectively for PAR710 and JSR AT111S (table 3).
roughness was found to be dependent on the PEB conditions. Higher PEB temperatures result in a decrease of the LER for the PAR710.

In summary, good lithographic performance (resolution, latitudes) is seen for the implementation on the gate level for logic design rules. Critical issues, which need further improvement, are PEB sensitivity and LER.

### 3.2 Study of illumination conditions

Conventional, annular or QUASAR™ illumination have been used to improve the processing windows for dense and semi-dense features. (QUASAR™ is ASML's proprietary quadrupole illumination mode, utilizing diffractive optical elements in combination with the AERIAL™ II illuminator). Figure 9 gives an overview of the illumination conditions used.

The process windows for 130nm dense, semi-dense (1.5 space/line ratio) and isolated lines were determined in each case. The experimentally determined process windows are shown in figure 10, showing exposure latitude versus depth-of-focus, as obtained from a rectangular box fitted into the ED windows. For dense 130nm lines, decent process windows are obtained using conventional illumination. The annular illumination setting shows a very similar process window, but the process window is significantly enhanced using QUASAR™. For semi-dense 130nm lines, very similar results are obtained for conventional and annular illumination again. Also here, QUASAR™ shows the best performance. For 130nm isolated lines, all three illumination settings show comparable performance.

When developing manufacturable processes, it is important not only to look at individual process windows but also to consider proximity effects. Figure 11 shows the results of the measured proximity effects for the three illumination cases. We plotted the required exposure dose versus pitch to print 130nm features 10% too small or too large. The height of the box fitted between these contours for a pitch range from semi-dense (space/line ratio of 1.5) to isolated lines is a measure for the overlapping exposure latitude for logic design rules. As can be seen, the fully 130nm dense lines all require a higher exposure dose and no overlap is found with the isolated lines over the full pitch range. For semi-isolated (space/line ratio = 1.5) to isolated lines, a small overlapping exposure latitude was found (see fitted box). For annular illumination, the curve looks very similar but the iso-dense bias is even larger. For QUASAR™ illumination, more oscillations are seen at intermediate pitches.
A special type of proximity effect is line-end shortening. It is generally known that very high resolution lines print shorter than designed and manufactured on the mask. Very often, line-end shortening is the first argument to start using optical proximity corrections. Obviously this makes the data preparation and mask manufacturing process more complicated and very likely more expensive. In figure 12, the line-end shortening of a 130nm isolated line is plotted against focus for the 3 illumination conditions. As can be observed, the line-end shortening is rather small and is lowest by the use of QUASAR™.

### 4. Implementation for the 130nm node

#### 4.1 130nm gate layer

**4.1.1. Polysilicon etch resistance**

The etch rate of several single layer resists has been tested in a typical polysilicon etch process in a LAM Alliance TCP9400PTX etcher. A polysilicon etch process consists of a breakthrough step using CF₄ chemistry, a main etch step using HBr/Cl₂ chemistry and finally an overetch step. The etch rate has been measured for a main etch process using HBr/Cl₂ and an etch time of 60 sec. In Fig. 13 the etch rate of several 193 nm resists is plotted relative to the etch rate of an I-line resist. Typical etch rates of 193 nm resists are a factor of 2 higher than novolac materials.

**Fig. 12:** Line-end-shortening for 130nm isolated line for three different illumination modes.

**Fig. 13:** Relative etch rate of 193 nm resists.

**Fig. 14:** Relative etch rate of 2nd generation 193 nm resist towards 1st generation resist.
In Fig. 14 the etch rate of the advanced materials such as Sumitomo PAR710 and JSR AT111S has been plotted relative to the Sumitomo PAR101 1st generation 193 nm resist. The acrylate based PAR710 resist has a comparable etch rate as the PAR101, however the JSR AT111S COMA type resist etches 20% slower.

Patterned polysilicon wafers have also been etched using Sumitomo PAR710 and JSR AT111S in combination with an 82 nm thickness organic BARC and in combination with a 24 nm SiON layer ARC material.

When using organic BARC as ARC a significant amount of resist has been consumed already during BARC etch. Therefore the amount of resist left after poly-Si etch might be marginal. However, when SiON is used as ARC, the etching of the SiON layer takes place during the breakthrough step of the poly-Si etch process and therefore no additional resist is consumed during ARC opening. As such the resist erosion by the poly-Si etch process is limited. After poly-Si etch about 130 to 150nm of resist is remaining on top of the etched polysilicon line for Sumitomo PAR710 and for JSR AT111S respectively.

Successful pattern transfer of 120nm lines into a 150nm thick poly-Si layer is demonstrated in Fig. 15 for JSR AT111S resist. Fig. 15 shows the 120nm semi-dense poly-Si lines after etch, before and after stripping of the resist. The resist consumption during etch is about 250nm. Also an excellent selectivity of the etch process is seen towards the 2.5 nm gate oxide. It can be concluded that despite the factor of two in etch resistance compared to novolac, the state of the art single layer 193 nm resists provide sufficient etch resistance for pattern transfer into a 150nm thick layer polysilicon layer.

An alternative to the single layer resist is to use thin layer imaging in a bi-layer approach where the imaging takes place in a thin (265 nm) top resist. The pattern of the top resist is then transferred into the 400nm thick bottom layer by dry development in an O2/SO2 plasma. Thin layer imaging systems have the potential for excellent lithographic performance and good etch properties. In a bi-layer approach, actually the organic bottom layer provides the dry etch resistance. Although it was not the intention in this work to do detailed comparison of single layer and bi-layer schemes, we did also tested the performance of the TIS2000 (ARCH chemicals) bi-layer resist in the poly-Si etch process. For a detailed lithographic analysis of the TIS2000, we refer to the literature [5-7].

By etch rate tests of unpatterned wafers, in an HBr/C12 plasma, it was found that the bottom layer etches a factor of 1.3 faster than I-line resists. On patterned wafers, >200nm of the underlayer is remaining after polysilicon etch when using the TIS2000 process.

The critical dimensions of a nominally 130nm line have been measured at three stages: after patterning of the top resist, after dry development of the bottom layer and after poly-Si etch. The actual depth of focus is significantly larger. A slight linewidth increase (6 nm) is seen by the dry development process, shifting the process window towards higher doses. By the polysilicon etch process, a decrease in linewidth of about 8 nm
was observed, shifting the process window back to lower doses. After polysilicon etching, 11.6% exposure latitude is obtained at 0.4µm DOF.

4.1.2 Patterning over topography
130nm gates at a minimum pitch of 300nm have been patterned over shallow trench isolation (STI) topography. Fig. 17 illustrates an excellent CD control over the STI topography over a 0.4 µm focus range for both organic BARC and inorganic BARC (SiON) as anti-reflective layer. Etching of the 150nm thick poly-Si gate layer was successfully done stopping on a 25Å gate oxide (Fig. 18).

Fig. 17: 130nm gates in JSR AT111S resist over STI topography after lithography.

Fig. 18: Etched 130nm shift-register cell after stripping of the resist.

4.2 130nm contact/via layer
Another critical layer for the 130nm node is the contact/via layer. Typically much thicker layers have to be etched as compared to the gate etch. For the 130nm node, we are focusing on 650nm thick oxide layers. As this is more demanding for the photoresist than the gate layer, we decided to coat the resist at 500nm thickness. For reflection control a 50nm SiON layer was applied underneath the oxide. Dedicated single layer contact hole resists as well as the TIS2000 thin imaging system, have been patterned on this substrate. 160nm contacts were exposed (0.63 NA, 0.4σ) using a binary mask and dry etched into the 650nm oxide using a LAM 4520XL platform in a C4F8 chemistry. The etched contact holes before stripping of the resist are shown in figure 19. About 220 m and 200nm resist is left on top of the oxide respectively for single layer resist 1 and resist 2. After oxide etching, a DOF of 0.6 µm was obtained on 160nm isolated contacts (Fig. 20).

Fig. 19: 160nm semi-dense (1:1.4) and isolated etched contact holes in 650nm oxide layer using resist 1 (a) and resist 2 (b) as masking layer.

Fig. 20: 160nm etched contact holes through focus before stripping of the resist (resist 2).

For the thin layer imaging approach (TIS2000), 160nm contact holes are shown after dry development of the bottom layer and after pattern transfer into the oxide layer in Fig. 21. Straight
sidewalls are obtained. Due to the higher dry etch resistance of the bottom layer, a significant amount of bottom layer (320nm) is remaining after oxide etch.

For via hole applications, a slightly different substrate is used. The SiON layer is on top of the oxide layer. Also here the single layer resists are performing well. Fig. 22 shows a 160nm and a 140nm etched via after stripping of the resist.

Fig. 22: 160nm and 140nm etched via holes

5. 193 nm for the 100nm node

Today, it is beyond doubt that 193nm will be the main technology for the 100nm node. Although resists have not reached full maturity yet and higher NA step and scan systems are expected for this, it is expected that strong enhancement techniques will be needed. Depending on the application, several candidates exist.

5.1 Alternating PSM

Alternating PSM are being used more and more today to push 248nm to its limits. In combination with double exposure techniques, phase assignment problems can be solved when trying to print gate layers\(^\text{11}\). A dark field 193nm alternating PSM was built with a light field trim mask and experiments were carried out in single layer resists. Since we focused on sub-130nm feature sizes, the resist thickness was reduced to about 330nm. Exposures were done using 0.63 NA and a fill factor of 0.32 using Sumitomo PAR710 resist. ED-windows have been measured for isolated lines and lines at a 0.25µm pitch. In figure 23, the exposure latitude in best focus and at 400nm/800nm focus depth is plotted for isolated and semi-dense lines of various sizes ranging between 60 and 100nm. Figure 24 shows cross-section micrographs of 70nm semi-dense and isolated lines through focus.

Fig. 22: 160nm contact holes in TIS2000 after dry development into the bottom layer (a) and after pattern transfer into the oxide layer (b).

Fig. 23: Exposure latitude in best focus and at 400nm and 800nm depth-of-focus for various sizes of isolated and semi-dense lines.

Fig. 24: Profiles of 70nm isolated and semi-isolated lines through focus (Sumitomo PAR710, 330nm thick)

643
window, as shown in figure 25. The aerial image contrast of these lines at 0.63 NA is comparable to the aerial image contrast of 100nm dense lines printed using 0.75 NA. These results hold promise that 0.75 NA ArF scanners will be able to print 100nm equal lines and spaces with large process windows.

6. Conclusions

In this paper, the status of ArF lithography has been reviewed, focusing primarily on the 130nm technology node. The lithographic performance of state-of-the-art 193 nm resists has been evaluated on optimized anti-reflective layers. Good lithographic performance has been demonstrated for the 130nm node on the current 193 nm full field scanners having NA's of 0.6. Critical resist issues are still line edge roughness and PEB sensitivity, which might limit the CD control. The effect of various illumination conditions on process windows and proximity effect have been illustrated.

Although the dry etch behaviour of 193nm resists is not yet comparable to 365nm or 248nm resists, it has been shown that the resists can already be used for integration in critical layers (gate and contacts) of typical CMOS processes. Based on these results and provided a further maturity of the resist process, it is expected that the higher NA (>0.70 NA) volume production ArF step&scan systems will be able to print the 130nm node without aggressive resolution enhancement techniques.

Initial results for the 100nm node using alternating phase shifting masks look very promising for 193nm, although a higher NA lens will certainly be needed here as well.

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8. References