Reduction of Multiple Interference Effect for Lithography

T. Koizumi, S. Kobayashi, M. Endo, M. Sasago, and N. Nomura
Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd.
3-1-1, Yagumo-nakamachi, Moriguchi, Osaka, 570, Japan

Abstract

To reduce critical dimension (CD) variation due to multiple interference effect, anti-reflective coating \(^1\) and over coating processes \(^2\) have been proposed and investigated. In this paper, we discuss the problem of the over coating processes and report a new and simple process, called OCT (Optical-path Control Technique), for reducing the multiple interference effect that does not require new material and equipment. CD variation can be reduced to 30% using OCT process. Furthermore, we discuss its application to an experimental 64MDRAM process.

1. Introduction

CD variation due to multiple interference effect has become a significant problem in LSIs fabrication below 0.5 micron design rule. In order to reduce the multiple interference effect, over coating process, anti-reflective coating process and dyed resist have been developed in g-line, i-line and KrF excimer laser lithographies. The dyed resist process is most simple, however, the resist pattern profile, the resolution and the depth of focus are degraded. The anti-reflective coating process is complicated and the removal of the anti-reflective material causes CD loss. The over coating process is also simple and effective for reduction of multiple interference effect. However, changes in film thickness of as small as 10nm from the optimized value can lead to significant deterioration in the reduction effect. \(^3\)

In this paper, we discuss the problem of the over coating process and propose a new technique called OCT (Optical-path Control Technique) for reducing multiple interference effect. In this technique, the exposure time is divided into two times with a baking process introduced between the first and second exposure. This procedure does not require any new material or equipment change. We report on the use of OCT to reduce multiple interference effect in a 64MDRAM process.

2. Over coating process

2-1. Concept
The multiple interference effect is caused by incident and reflective light rays from substrate and resist surface, as shown Fig.1. The over coating process reduces the reflective light from resist surface. Figure 2 shows the concept of the over coating process. An over coating material is coated on resist at $\lambda/4n$ thickness ($\lambda$: wavelength of exposure light, $n$: refractive index of the over coating material for $\lambda$). The optimum of $n$ is determined as $\sqrt{N}$ ($N$: refractive index of the resist for $\lambda$). Reflective light from interface between air and the over coating film (Lo) interferes with reflective light from interface between the over coating film and the resist (Lr). Phase of the Lo in resist is 180 degree different from the Lr because the over coating film thickness is $\lambda/4n$. The reflective light from resist surface, in other words, the multiple interference effect is reduced or disappear.

2-2. Experiments and results

As an over coating material, polyvinyl alcohol is adopted because it is water-soluble and has low refractive index. The water-soluble material is simultaneously removed with resist development, so it simplifies the lithography process. We applied this technique to KrF excimer laser lithography. The index of refraction of the over coating material for 248nm is 1.46. The optimum thickness for 248nm is 42nm.

Resist used in these experiments is ASKA, which is our in-house developed chemically amplified positive resist for KrF excimer laser lithography. First, the resist is spin-coated on substrate with HMDS treatment and baked on a hot plate at 90°C for 90sec. Resist thickness is varied from 0.95micron to 1.03micron. Then, the over coating material is spin-coated on the resist. The exposure is done by KrF excimer laser stepper with 0.42 NA lens, and post exposure bake is done at 95°C for 90sec. Finally, development is done by TMAH solution. At the same time, the over coating film is removed because it is water-soluble.
Figure 3 shows line width variations versus resist thickness variation with and without the over coating film. Mask pattern is 0.35micron line and space patterns. Exposure energy without the over coating film was 28mJ/sq.cm and one with the over coating film was 26mJ/sq.cm. This results indicate that the resist sensitivity is independent on the developed over coating material. The line width between top and bottom of variation curve is defined as $\Delta L$. The $\Delta L$ without the over coating film is 0.13micron. On the other hand, the $\Delta L$ with the over coating film is 0.045micron. The multiple interference effect using the over coating film is reduced down to 65% of one without the over coating film.

![Line width variations versus resist thickness variation](image)

$0.35\mu m \ L/S$

Figure 4 shows $\Delta L/2$ variations versus the thickness variation of over coating film. The thickness of the over coating film is varied from 42nm to 84nm. This thickness variation is corresponded from the optimized thickness($\lambda /4n$) to the most ineffective thickness for 248nm. Mask pattern is 0.35micron line and space patterns. When the thickness of the over coating film varies 50%, which corresponds to about 20nm difference from the optimized thickness, multiple interference effect is not reduced. In order to reduce the line width variation to 10% of 0.35micron, the thickness variation of over coating film must be within 20% of the optimized thickness.

The thickness of the over coating film can not be controlled by the resist coating process on topographic substrate. In this case, the reduction of multiple interference effect is not sufficiently obtained, because the thickness variation of the over coating film becomes distinct. This is the critical problem of the over coating process. In order to resolve this problem, we have developed new simple process called OCT.

3. OCT process

3-1. Concept and Process of OCT
Figure 5 shows the concept and the process sequence for OCT. First, the spin-coated resist on a substrate is exposed at under the 1st optimum energy. Next, the resist is shrunk $\lambda/4n$ in thickness by baking. This baking step is named shrink bake. Then, the resist is exposed at under a 2nd optimum energy again. Finally, the resist is developed. The multiple interference effect of the second exposure becomes just the opposite to the first exposure because the resist thickness is changed $\lambda/4n$ by the shrink bake. Accordingly, the absorbed exposure energy in resist is even at each resist thickness through the control of the optical-path, reducing CD variation drastically. It is
easy for developed OCT process to control resist thickness change for obtaining multiple interference reduction effect because the resist thickness is changed by baking process.

3-2. Experiments

It is important to optimize the ratio of 1st to 2nd exposure energy in the OCT process. Figure 6 shows the line width of 0.5micron isolated pattern and 0.5micron SRAM cell pattern on the same CMOS chip as a function of the ratio 1st to 2nd exposure energy. This process is adapted to i-line lithography. The i-line positive resist used in these experiments was PFR-IX061 (Japan Synthetic Rubber Co., Ltd.). The conditions of pre-bake, shrink bake and post exposure bake were at 80°C for 90sec, at 115°C for 120sec, at 115°C for 120sec, respectively. The resist thickness variation by the shrink bake was 54nm, which is approximately \( \lambda/4n \) (\( \lambda =365\text{nm}, n=1.68 \)). However, line width of the isolated pattern was different from SRAM cell pattern due to multiple interference effect. Therefore, the difference between the line width of both patterns become the minimum at the optimum ratio of energy. The optimum ratio of 1st and 2nd exposure energy for this resist was 4 to 1.

3-3. Results

Figure 7 shows the multiple interference effect, which is the variation of the line width versus the resist thickness change, for a 0.5micron line and space pattern for conventional and OCT processes on Si substrate. The OCT process can reduce the line width variation down to about 30% of the conventional process.

One would expect a deterioration of CD control by the OCT process due to alignment accuracy between two exposures. Figure 8 shows the line width of 0.5micron pattern versus alignment
offset between 1st and 2nd exposure. The line width hardly varies even if the alignment offset became 0.3micron. Figure 9 shows the measured results of the line width variation in OCT process. The negligible small alignment error using the same alignment mark may result in negligible line width variations. The alignment error between 1st and 2nd exposure can be neglected.

3-4. Application to 64MDRAM pattern

Figure 10 shows the line widths of the center and 4 corners in whole cell patterns of 0.35micron rule 64MDRAM. The resist thickness of center is different from that of corner. The line width variation between the center and 4 corners is about 0.1micron for conventional process. On the other hand, the variation is reduced to 0.04micron by for OCT process as shown in Fig.10.

Figure 11(a), (b) show SEM photographs of 64MDRAM cell pattern at a corner. We can clearly observe the improvement in pattern shapes by using OCT process.
4. Conclusion

An over coating process is simple and can reduce multiple interference effect. From the results, line width variation is reduced down to 65% of one without the over coating process. However, if the over coating film varies 50%, which corresponds to about 20nm, the multiple interference effect is not reduced. Accordingly, this process has the serious problem of delicate thickness control of the over coating film on topographic substrate.
To resolve this problem, we have developed new simple process called OCT (Optical-path Control Technique). It is easy for developed OCT to control resist thickness change for obtaining multiple interference reduction effect because the resist thickness is changed by baking process. The developed process can very reduce line width variations due to multiple interference effect. The line width variation is reduced to 30% when compared with a conventional process. It is shown that the alignment accuracy between 1st and 2nd exposure does not affect the line width variation. This process is a very promising process technology on any exposure wavelength for reducing multiple interference effect and can be successfully applied to topographic processes for 64MDRAM.

Acknowledgments

The authors thank Dr.Y.Tani, Dr.K.Yamashita, and the technical staff of VLSI Technology Research Laboratory for their useful discussions and cooperation. The authors also thank Dr.T.Takemoto and Dr.M.Inoue for their encouragement and support on this work.

References