DEVICE MINIATURIZATION AND LITHOGRAPHY IN GIGA-BIT-ERA DRAMs

TORU KAGA
Central Research Laboratory, Hitachi, Ltd.
Kokubunji, Tokyo 185, Japan

There is no physical limitation to giga-bit era DRAMs. Continuing miniaturization of DRAM cells will require smaller minimum feature size, the very good alignment tolerance of less than 20% of the minimum feature size, and a higher aspect-ratio resist system, the keys to the high-density DRAMs of the future.

1. Introduction

DRAM cells lose about 2/3 of their area with each successive generation, according to Fig. 1, where all data points refer to ISSCC (International Solid-State Circuits Conference) papers. This miniaturization has continued through 256 mega-bit generation [1,2,3] and could continue into the future if lithography continues to improve resolution. However, there are several issues involved in making very small DRAM cells:

(1) Can small DRAM cells still store enough charge to overcome the noise charges such as alpha-particle-oriented, circuit noise, etc.?
(2) What kind of DRAM cell structure will appear in the giga-bit era?
(3) How will these new types of cells affect lithography?

![Fig. 1 Trends in chip area and memory cell area of DRAMs](image-url)
This paper will discuss the required electrical characteristics of DRAM cells and their structure in the giga-bit era and consider the above issues.

2. DRAM cells in giga-bit era

(1) Trend in DRAM cell area

The miniaturization of DRAM cells by about 2/3 each generation has been maintained through the reduction of feature size, which has been accomplished by improving lithographic resolution. Here, I assume that this miniaturization will continue in the future.

(2) Trend in power-supply voltage

The miniaturization of DRAM cells requires the reduction of the power-supply voltage because electrical reliability must be maintained in scaled DRAM devices. The reduced power-supply voltage \( V_{cc} \) also reduces stored charges \( Q_s \) of a DRAM-cell capacitor because

\[
Q_s = C_s \times V_{cc}, \tag{1}
\]

where \( C_s \) is the capacitance of the DRAM capacitor. However, the stored charge \( Q_s \) must overcome the noise charges. The main job of DRAM designers, hence, is to increase the capacitance \( C_s \). (This will be discussed later.)

Changes in the power-supply voltage \( V_{cc} \) of DRAMs are shown in Fig. 2, where all data points refer to ISSCC papers. The low power-supply voltage era started with the advent of 16-mega-bit DRAMs, which marked the ending of the long 5-V power-supply voltage era. This change is mainly
due to electrical reliability problems in scaled devices. In addition, the low power-supply voltage is thought fitting for the "Green Electronics" revolution because the power dissipation \( P \) of a circuit reduces according to the following equation:

\[
P = \frac{V_{cc}^2}{R},
\]

where \( R \) is simplified circuit resistance. Thus, power-supply voltage reduction may spur progress in the future giga-scale DRAM era.

(3) Trend in stored charge in a DRAM cell

The required stored charge \( Q_s \) of a DRAM cell against alpha-particle injection is also constantly reducing, as shown in Fig. 3, where all data points refer to ISSCC papers and \( Q_c \) is the measured critical stored charges against alpha-particle injection [4]. Here, all \( Q_s \) values exceed \( 1.5Q_c \), that is, \( Q_s \) has a margin of 50% more charges than the \( Q_c \). Trends in \( Q_s \) and \( Q_c \) show a constant reduction in the ratio of about 70% each generation. This reduction rate is almost the same as that of the minimum feature size of DRAM cells. This coincidence comes from the relation between the collected charges caused by alpha particle injection and the depletion layer width under a DRAM cell. That is, the charges are almost linearly dependent on depletion layer width [5] and the depletion layer width is approximately proportional to the minimum feature size of the cell. The stored charges in giga-bit era DRAM cells, therefore, must exceed the value of \( 1.5Q_c \) in Fig. 3.

(4) Features of giga-bit era DRAM cell's

Table 1 summarizes the features of giga-bit era DRAM cells. These values are obtained by extrapolation of data in Figs. 1, 2, and 3.

<table>
<thead>
<tr>
<th>BITS</th>
<th>64M</th>
<th>256M</th>
<th>1G</th>
<th>4G</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN. F. SIZE (( \mu m ))</td>
<td>0.3</td>
<td>0.2</td>
<td>0.13</td>
<td>0.08</td>
</tr>
<tr>
<td>CELL AREA (( \mu m^2 ))</td>
<td>1.6</td>
<td>0.58</td>
<td>0.21</td>
<td>0.08</td>
</tr>
<tr>
<td>INT. Vcc (V)</td>
<td>2.5</td>
<td>2.0</td>
<td>1.5</td>
<td>1.2</td>
</tr>
<tr>
<td>( Q_s ) (fC) [1.5xQc]</td>
<td>32</td>
<td>22</td>
<td>15.5</td>
<td>11</td>
</tr>
<tr>
<td>( Q_s ) (fF)</td>
<td>26</td>
<td>22</td>
<td>21</td>
<td>18.5</td>
</tr>
</tbody>
</table>

The cell area of 1 giga-bit DRAMs is 0.21 \( \mu m^2 \) and that of 4 giga-bit DRAMs is 0.08 \( \mu m^2 \). Their respective minimum feature sizes are 0.13 \( \mu m \) and 0.08 \( \mu m \). These values may be aggressive in the development stage, but might be reasonable in the mass-production stage.
The internal power-supply voltages $V_{CC}$ of 1 giga-bit DRAMs and 4 giga-bit DRAMs applied to memory cells are 1.5 V and 1.2 V, respectively. On the other hand, the required stored charges are $15.5 \, fC$ and $11 \, fC$. We can calculate the capacitance values $C_s$ for 1 giga-bit DRAM cells and 4 giga-bit DRAM cells as $21 \, fF$ and $18.5 \, fF$, respectively. The calculated $C_s$ values are almost constant because both the minimum feature size and the $Q_s$ decrease almost simultaneously.

By using these values, we can estimate the equivalent insulator thicknesses $T_{eff}$ for these DRAM cells. Here, $T_{eff}$ is the thickness calculated using

$$T_{eff} = \left( \frac{\varepsilon_{SiO_2}}{\varepsilon_i} \right) T_i, \quad (3)$$

where $\varepsilon_{SiO_2}$ is the permittivity of SiO$_2$ and $\varepsilon_i$ is the permittivity of insulating films, and $T_i$ is the thickness of the films.

![Fig. 4 Relationship between equivalent insulator thickness and cell area or capacitor area in giga-bit DRAM cells](image)

Figure 4 shows the results of calculations, where the equivalent insulator thicknesses $T_{eff}$ are shown as a function of the capacitor area of a cell. Here, the capacitor area has a lateral extent on right and left of the memory-cell area. This is because the capacitor area varies with the structure of the capacitor, that is, a simple stacked capacitor cell (STC) has a capacitor area of about $1/3$ to $1/2$ of its cell area, on the other hand, a three-dimensional new-age cell (discuss later) has a capacitor area of about 3 or more times its cell area.

As shown in the figure, the required equivalent insulating thickness for the 1 giga-bit DRAM cell with simple STC is about $1 \, nm$, and for the three-dimensional cell, about $0.2 \, nm$. Those for a 4...
giga-bit DRAM cell are also calculated as 0.3 nm and 0.05 nm. Conventional Si₃N₄-compound films can no longer be applied to these DRAM cells because of their poor sustainable voltages. New insulating films such as Ta₂O₅, SrTiO₃ and PZT are required.

An important condition for these films is

\[ Q_s \leq Q_{\text{max}} = C_S \times V_{\text{max}}, \quad (4) \]

where \( Q_{\text{max}} \) is the maximum stored charge and \( V_{\text{max}} \) is the sustainable voltage of the films, because \( Q_s \) does not exceed \( Q_{\text{max}} \). We can transform Eq. (4) into the following equations:

\[ Q_s \leq Q_{\text{max}} = \varepsilon \varepsilon_0 \times S \times V_{\text{max}}/T_1, \quad (5.1) \]

\[ = \varepsilon \varepsilon_0 \times S \times E_{\text{max}}, \quad (5.2) \]

where \( \varepsilon \) is the relative permittivity and \( E_{\text{max}} \) is the sustainable electric field of the films. We experimentally found a relationship between \( E_{\text{max}} \) and \( \varepsilon \), as shown in Fig. 5.

Here, \( E_{\text{max}} \) is in proportion to \( \varepsilon^{-0.5} \). By combining this result and Eq. 5.2, we can obtain

\[ Q_s \leq Q_{\text{max}} \propto \varepsilon^{0.5}. \quad (6) \]

The larger \( \varepsilon \) becomes, the larger \( Q_s \) becomes. Introduction of high-\( \varepsilon \) materials, therefore, is the good way to achieve giga-bit era DRAMs.

(4) Trend in DRAM cell structure

The evolution of DRAM cell structures is shown in Fig. 6.
As shown in the figure, the planar cell structure used until the early mega-bit era was replaced by the stacked capacitor type (STC) or the trench type. The STC type cell has been recently modified to the multi-cylinder type or the multi-fin type. A rugged surface has also been introduced for enlarging their surface areas. The future structure of STC cells may be the ferro-electric type because the area-enlargement methods shown in the figure approach the limit.

The other way to enlarge the surface area of capacitors is to use trench capacitors. In this category, the substrate-plate-type cells and the stacked-trench-type cells have been introduced. However, it is very difficult to use ferro-electric films in the trench-type cells because the ferro-electric materials contain heavy ions that make it difficult to deposit these materials directly on the Si surface. In the trench-type cells, the choice of the SOI (silicon on insulator)-plus-trench capacitor structure may be the better way to make giga-bit era DRAMs because this gives the maximum capacitor layout in the limited cell region.

3. Giga-bit era DRAM cells and lithography

First, for the discussion in this section, I assume STC as a giga-bit era DRAM cell. This is because the STC has a very high aspect ratio, which is harmful for the lithography. If lithography engineers can solve the problem, the same technology can easily be applied to the trench-type cells.
(1) Alignment tolerance

All types of memory cells require alignment tolerance because this can eliminate misalignment problems between two adjacent patterns. The alignment tolerance, however, increases cell area, as shown in Fig. 7. The figure shows the relation between relative cell area and the alignment tolerance.

We used a simple STC structure as a reference in considering this problem. A simplified structure layout was assumed; that is, we used the minimum feature size for all patterns and we used the same space for all alignment tolerances. As shown in the inset, we can express the cell area as follows:

\[
\text{(cell area)} = (\text{lateral cell size}) \times (\text{vertical cell size}), \quad (7.1)
\]

\[
= (4F + 3X)(2F + 2X), \quad (7.2)
\]

where \( F \) is the minimum feature size and \( X \) is the alignment tolerance. So, if we want to reduce the cell area to less than 50% more than the area of the ideal smallest cell, the alignment tolerance must be less than about 20% of the minimum feature size of the cell.

(2) Aspect ratio of DRAM cells

One problem with the STC is increasing cell height: DRAM designers want to increase the height to enlarge the effective capacitor-area of the cell. Figure 8 shows the trend in memory-cell height, where CUB is the name of the STC having a capacitor under its bitline (as in conventional STC) and COB is the name of the STC having a capacitor over its bitline.
The CUB structure has been used since 4-mega-bit mass production. It increased the height in the 16 mega-bit era. However, it reduced the height in the next generation because area-efficient capacitor structures such as the fin structure\cite{6} or the cylinder structure\cite{7,8} were introduced (see Fig. 6). The newer structure, COB, introduced in 16 mega-bit era, features its larger capacitor-area than CUB. All STC cells in 256 mega-bit DRAM's \cite{2,3}, therefore, used COB.

COB structures are classified into three groups, the smaller-cell-area self-aligned types (A) and (A') and the non-self-aligned type (B). Figure 9 clearly shows the difference among these, where the ordinate shows the normalized cell height calculated using the following equation:

\[
\text{(normalized cell height)} = \frac{\text{(memory cell height)}}{\text{(minimum feature size)}}
\] (8)

As shown in the figure, the self-aligned cells (A) and (A') are higher, but they have larger effective capacitor-areas in the smaller cells than the non self-aligned type (B). A common issue in all types of the COB cells is increasing normalized cell height. Higher-aspect-ratio resist patterns thus will be needed in giga-bit-generation DRAMs.
4. Conclusion

Main memory (mainly DRAM) demand in the electronics industry is expected to continue to increase in the future because people's desire is unlimited, that is, we want much more user-friendly human interfaces and much faster computers. Thus, increasingly complicated operating systems have been developed, as shown in Fig. 10. To meet the likewise-increasing memory requirements, we will have to develop much higher-density DRAM chips in the future.

Maintaining performance of these continuously miniaturizing DRAM cells requires ever-smaller minimum feature size, very good alignment tolerance of less than 20%, and a higher-aspect-ratio resist system. These are the keys to the future fabrication of high-density DRAMs.

References


