FUTURE TREND OF LOGIC DEVICES AND REQUIREMENTS TO LITHOGRAPHY

KENJI MAEGUCHI

Semiconductor Device Engineering Laboratory
Microelectronics Engineering Laboratory
Toshiba Corporation, Kawasaki, JAPAN

1. Introduction

High-performance workstation, personal computer and consumer electronics products are now requiring the advanced silicon process technology as a means of integrating entire system onto a single chip. The leading-edge workstations demand the continuous performance improvement of microprocessors. The future multimedia products will be portable. This poses severe constraints on power and cost. MOSFET miniaturization and increased interconnect density are required to realize the high performance and highly integrated logic LSIs with lower power and lower cost. Further improvement in lithography is much more indispensable to future logic devices.

Fig.1 Trends of Speed and Integration
Density in Microprocessors

2.Logic devices trend

2.1 Microprocessors

High performance RISC processors are operating at 75-100MHz externally and achieving 100SPECmark computing power(Fig.1, Fig.2).[1] New pentium processor integrates 3.3million transistor, and operates at 100MHz.[2] To achieve the high performance, designs have to be optimized totally, which include architectural design, logical and physical design. In addition, high speed on-chip cache memory technology is indispensable to realize more computing power. External clock frequency will be increase 10 times over 10 years. Continuing device miniaturization from half-micron is strongly required. Processors will be divided into three groups(Fig.2). One is the very high performance computer applications, which performance is a key consideration. Second is desktop WS and PC applications, which cost/performance is key factors for the market. Third is the portable computer and communication applications, for which power consumption must be kept to a minimum. Technologies of high-end microprocessors penetrate to low-end which include desktop WS, PC and portable PC. Portable information electronics such as PDA need extremely low power consumption for battery operation.

Fig.2 Power and Performance of Microprocessors

Fig.3 Performance and Design Rule Trends of Video (De)Compression LSIs

2.2 Multimedia LSIs

In multimedia services, including speech, graphics and video, video compression is a vital technology for such markets as video conferencing, video on demand and next generation entertainment. Progress in silicon technology has enabled a single-chip MPEG (Motion Picture Experts Group) 2 video decoder LSI, which decodes bitstreams of CCIR601 (720x480) resolution in real-time. [3] Fig. 3 shows the performance to be needed for several video compression standards and also the expected metal design rules to realize the single-chip integration. In future, decoder/encoder chip with HDTV (1440x960) standard can be realized at reasonable chip size by continuing Si technology progress. Recently, high silicon performance and gate integration are ready to design a DSP (Digital Signal Processor) at 1GOPS range. General purpose DSP can perform multiple tasks due to its software programmability. The DSP system can run alternative programs when a new function or standard were needed. The DSP will become the important technology in multimedia system such as a multimedia WS/PC. Multimedia products will be portable. Then extremely low power consumption have to be realized for battery operation.

2.3 Device technology

There is no fundamental obstacle to continue the device miniaturization to 0.1 micron range. The miniaturization is accelerated to achieve the high performance, low power and low cost logic LSIs. The power/performance trade-off is becoming an important issue. Low voltage operation is the key to reduce the power consumption. To enable the low voltage operation without sacrificing performance, how to realize the low V_{th} of MOSFETs is the most biggest problem. Thin film SOI is the one candidate to get the extremely low V_{th} . Parasitic resistance and capacitance on MOSFETs and interconnections are the another difficult problem to be solved. New technologies such as salicide structure, Cu interconnection and low dielectric constant insulator will be applied in future. Package design is increasingly important in system applications. Though the single-chip packages will be continue to dominate the chip package, the leading-edge workstations and consumer portables require MCM technology from high performance and low cost, respectively. Known good die (KGD) technology and infrastructure problems must be solved.

	1991	1994	1997	2000	2003
Feature Size					
Gate Length (μm)	0.5	0.35	0.25	0.15	
Metal D.R. (μm)	0.8	0.6	0.35	0.25	
No. of Interconnect	3	4 / 5	5	5 / 6	
Chip Size (mm^2)	250	350	550	800	
Transistors / Chip	1.5 M	3.0 M	6.5 M	20 M	
Resolution (μm)	0.5 ($<\pm 0.05$)	0.35 ($<\pm 0.03$)	0.25 ($<\pm 0.02$)	0.15 ($<\pm 0.01$)	
Overlay (μm)	0.15	0.12	0.08	0.05	
Depth of Focus (μm)	Depend on device topography and manufacturing margin.				

Fig.4 Logic Technology Roadmap and Requirements to Lithography

3.Requierments to lithography

Logic technology roadmap and requirements to lithography for the next ten years are summarized in Fig.4. Logic roadmap requires the evolution in minimum feature size from today's 0.5 micron to 0.15 micron. We can expect to have a 20million transistors chip with five- or six-layers of metal about the year 2000. The process will use a gate oxide thickness of 40 Å. The supply voltage will fall from 3.3V to 1.5V. MOSFET miniaturization is now driven by a leading edge device such as a high performance microprocessor. Performance is directly proportional to drive current capability of CMOSFET and inversely proportional to parasitic capacitance, resistance. Gate length reduction is the key to get the performance improvement. In order to achieve the highest performance, gate length of the microprocessor is already beyond memory (Fig.5). [4] Microprocessor requires strongly the improved line resolution and precise control across the increasing chip area. In comparison to memory with regular patterns, logic have a feature of random patterns including isolated lines. This requires the very difficult technical challenge in lithography. New technologies such as a phase shift mask must take the random patterns peculiar to the logic into consideration. In addition, measurement methods must be improved to control the lithography process with critical dimensions less than 0.5 micron.

Critical paths of high performance LSIs are often long interconnection. This needs the advanced metal system. And the integration density in logic LSIs are limited by multi-level metal pitch. Logic LSIs are designed by gate arrays, cell-based, full-custom design methods. Those use mostly automatic place and route tools. This requires the same metal pitch with lower level for higher levels, borderless/stacked contacts. Fine-pitch metal design with large topographic feature heights call for improvement in resolution, overlay and depth of focus. Of course, process technology improvement such as a contact plug, CMP (Chemical Mechanical Polishing) and anti-reflection coatings over metal should be done simultaneously.

From manufacturing standpoint, multigeneration and low-cost exposure system are needed to drive cost reduction. Customer calls for the quick Turn-around-time (TAT). TAT of mask making and mask inspection are important, especially AS IC LSIs.

Fig.5 Gate Length Trends of DRAM, MPU

4.Summary

The rapid performance improvement being made in microprocessors, video compression and so on will open up the multimedia environments near future. Higher performance, lower power and lower cost requirements in leading-edge logic LSIs push the MOSFET miniaturization and fine multi-level interconnection beyond DRAM. This requires the lithography improvement more and more. Fine line resolution/control will be one of the most difficult technical challenge in lithography. These technical challenge should be solved from the total process optimization standpoint, which include the unit process and process integration.

References

1. N. Ikumi, et al., ISSCC Digest of Technical Papers, pp.204-205, Feb., 1994.
2. J. Schulz, ISSCC Digest of Technical Papers, pp.202-203, Feb., 1994.
3. T. Demura, ISSCC Digest of Technical Papers, pp.72-73, Feb., 1994.
4. S. Kohyama, to be published.