X-RAY LITHOGRAPHY -RECENT PROGRESS AND FUTURE PROSPECTS-

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An overview of the present status of synchrotron radiation-based x-ray lithography (SRL) and its extendibility down to 0.1-micron features and lower are described. The attained performance of SR sources, aligners, and masks is measured with requirements for 1Gb DRAM level. Some of SR sources so far developed can provide enough SR flux for practicable throughput. While several prototype aligners have demonstrated sufficiently high alignment accuracy, the mask pattern placement needs to be further improved in order to fulfill the overlay requirement. The resolution well below 0.1 micron is feasible with narrow proximity gap of order of 10 micron. Difficulties in fabricating fine pattern masks can be reduced by making use of the phase shift effect. Investigation on the mask membrane deformation during stepping with the narrow proximity gap is now in progress.

1. Introduction

The current evolution of ULSI toward gigabit-scale integration requires advanced lithography with extremely high performance. Although improvement of optical lithography has been intensively pursued, production-viable technology for feature sizes less than 0.2 micron has not been established as yet. ArF excimer laser (193 nm) lithography is taken to be the most desirable candidate for the 0.18-micron generation. However, essential components, such as practicable exposure tools, damage-free optical material, and optimized resists, are not available at present. The necessity of a development program was only just proposed at the last SPIE Symposium[1].

Synchrotron radiation-based proximity X-ray lithography (SRL) is the most promising alternative to the optical means because of its excellent lithographic performance. SRL can provide simple and robust processes, as well as precise linewidth control. This will become more and more important with increase of integration density and complexity of ULSI devices.

The essentials of SRL have almost established and the compatibility with

ULSI processes has been demonstrated by fabrication of various devices, e.g. 0.2-micron-level CMOS devices[2], 512k SRAM with 0.25-micron gates[3], and 64 Mb DRAM[4]. What is required for SRL hereafter is to upgrade the overall technology for 1 Gb DRAM level. Another important concern is the extendibility down to 0.1-micron features and below, which will promise the applicability of SRL over several generations of ULSI.

In this article presented are an overview of the current status and the future possibilities of SRL. Especially, the achieved performance of major key technologies including SR sources, aligners, and masks is described. Technical issues and possible approaches to extend SRL down to 0.1-micron region are also described.

2. R&D activities

Figure 1 shows a schematic view of the SRL system of our laboratory. Almost all components are different from the conventional optical ones and thus need to be newly developed. R&D activities based on a dedicated SRL system are summarized in Table 1. The predecessor of Fraunhofer-ISiT (IMT: Institut für Mikrostrukturtechnik) is one of the pioneers in SRL. The proposal of COSY[5] stimulated the development of compact storage ring in Japan. Recent activities in Europe including those of ISiT and L2M (Laboratoire de Microstructures et de Microelectronique) appear to be addressed to new fields, such as microsystem technology and nanolithography, rather than development of manufacturing-viable SRL technology.

The largest activities in USA is based at IBM ALF (Advanced Lithography Facility) in East Fishkill, which is "Center of Excellence (CoE)" conducting ALP (Advanced Lithography Program) supported by ARPA (Advanced Research

Fig.1 Schematic view of the SRL system at SORTEC Laboratory.

Table 1 SRL activities

Institution/Facility	SR Source		Magnet Type	Aligner	(Fabricator)
	Name	Energy (GeV)			
<u>Europe</u>					
Fraunhofer-ISiT	BESSY	0.8	Normal	XRS-200	(Karl Suss)
L2M	Super-ACO	0.8	Normal	XRS-200	(Karl Suss)
<u>USA</u>					
IBM East Fishkill/ALF	HELIOS	0.7	Super	XRS-200	(Karl Suss)
Univ. Wisconsin/CXrL	ALADDIN	1.0	Normal	XRS-200	(Karl Suss)
<u>Japan</u>					
NTT/LSI Lab.	Super-ALIS	0.6	Super	SS-1	(in-house)
SORTEC	-	1.0	Normal		(Matsushita Elec.)
Mitsubishi Elec. Ind.	-	0.6	Super	XRS-200,	?(CANON)
Toshiba (NTT/LSI Lab.)	NAR	0.8	Normal	TOXS-1	(in-house)
Sumitomo Heavy Ind.	AURORA	0.575	Super	SATELLITE	(in-house)

- ★ ISiT: Institut fur Silziumtechnologie
 L2M : Laboratoire de Microstructures et de Microelectronique
 ALF : Advanced Lithography Facility
 CXrL: Center for X-ray Lithogagraphy
 NTT : Nippon Telegraph and Telephone Corporation
 Super: Superconducting Normal: Normalconducting

Projects Agency). Semiconductor manufacturers, such as IBM, AT&T, Motorola, and Loral Federal Systems are collaborating in application of SRL to device fabrication. The ARPA's program also includes development of infrastructure, such as high throughput aligners, new resists, a national mask shop, mask defect inspection and repair machines, etc. Another CoE is CXrL (Center for X-ray Lithography), where rather fundamental approaches are being conducted under collaboration between academy and industry.

In addition to those listed in Tab.1, there are not a few activities in Japanese industry, most of which are mainly addressed to mask making technologies. While the US activities seem to be well aligned with the purpose to promote insertion of SRL into industry, those in Japan are somewhat diverging and lacking in strategy for technology integration. The project of SORTEC, which is a consortium of 13 private sector companies, is scheduled to terminate next March. NTT LSI Laboratory is expected to be Japanese CoE thereafter.

3. SR source

3.1 Current status

For a production-viable SRL system, a compact and low cost electron

Table 2 Compact Electron Storage Ring Developed for SR Lithography

Machine	Institution	Electron Energy (GeV)	Critical Wavelength (nm)	Footprint (m ²)	Current Achieved (Max:mA)	Lifetime (h) (at mA)
<u>Superconducting Magnet Type</u>						
COSY	Fraunhofer-IMT	0.59	1.2	5×2	1	
HELIOS	Oxford Instruments	0.7	0.845	6.0×2.5	300	20 (200)
AURORA	Sumitomo Heavy Ind.	0.575	1.47	3φ	600	17 (300)
SUPER-ALIS	NTT LSI Lab.	0.6	1.7	8.8×2.5	500	5 (500)
NIJI-III	ETL/Sumitomo Elec.	0.6	1.3	6×4	200	4 (200)
-	Mitsubishi Elec. Ind.	0.6	1.5	6×3	300	
<u>Normalconducting Magnet Type</u>						
LUNA	Ishikawajima Heavy Ind.	0.8	2.2	8×8	80	5 (50)
NAR	NTT LSI Lab.	0.8	2.0	17φ	120	5 (120)
-	SORTEC	1.0	1.55	15φ	500	80 (200) 25 (500)

★ IMT : Institut fur Mikrostrukturtechnik
 NTT : Nippon Telegraph and Telephone Corporation
 ETL : Electrotechnical Laboratory

storage ring is required as an SR source. Table.2 shows major parameters of SR sources developed for lithography use[5-10]. HELIOS is the first compact ring introduced on the commercial basis. It has been routinely operating at the IBM ALF since the beginning of 1992, exhibiting high uptime close to 100% and good performance exceeding the designed specifications[11]. The SR ring of our laboratory has also achieved high performance, such as long lifetime of 25 hours, large stored current of 500 mA[12], and uptime over 98% during last 12 months. Almost all other rings have achieved the designed performance and are being routinely used in the respective laboratories. It seems that there is no fundamental problem concerned with the design concept and stable operation of the SR sources.

3.2 Evaluation of throughput

In ULSI production, high throughput is one of the most important requirements, since the throughput directly affects the lithography cost. Throughput TP (wafers/hr) is given by the following equation,

$$TP = 3600 / \{T_{oh} + N(T_e + T_s)\},$$

where T_{oh} is the overhead time for wafer exchange and global alignment, N the number of exposure fields per wafer, T_s the time for stepping, settling, and fine alignment per field, and T_e the exposure time per field, which depends on

the resist sensitivity S and the exposure intensity P_e as follows,

$$T_e = S/P_e.$$

The wafer size and the field area are assumed 12 inches diameter and 32 mm square (2 chips/field), respectively, and hence $N=60$. If $T_{oh}=30$ sec, $T_s=0.5$ sec, and $T_e=1$ sec, throughput is 30 (12" wafers/hr). This value is well comparable with 60 (8" wafers/hr). Since resists with sensitivity equal to or even less than 100 mJ/cm^2 are feasible, $P_e=100 \text{ mW/cm}^2$ is enough for $T_e=1$ sec. If the stored current is 500 mA and the beamline transmittance is enhanced by several times by using a flux-collecting mirror, $P_e=100 \text{ mW/cm}^2$ can be attained.

In practical use, loss of throughput due to the decay of the stored current should be taken into account. The storage ring of our laboratory which employs a full energy injection scheme can be operated with nearly constant current within $\pm 1\%$ variation by automatically refilling additional electrons[13]. On the other hand, almost all compact rings shown in Tab.2 adopt the low energy injection scheme to reduce the geometrical size and the injector cost. In this case, it is necessary to interrupt the current storage in order to recover the current by refilling, as shown in Figure 2.

When the vacuum of the storage ring is well aged and thus the lifetime of the stored current is mainly governed by SR-stimulated gas evolution from the vacuum wall, the lifetime is inversely proportional to the stored current. This is actually observed with the SORTEC ring as shown in Figure 3. In this case, the decay of the stored current is,

$$I/I_1 = 1/\{1+(e-1)t/\tau\},$$

Fig.2 Decay with time and recovery by refilling of stored current.

Fig.3 Dependence of lifetime on stored current.

where I_i is the initial stored current at $t=0$, τ the lifetime for $1/e$ decay, and t the time after the start of operation.

The exposure time is given by,

$$T_e = T_{ei} / (I/I_i),$$

where T_{ei} is the exposure time at $t=0$.

Figure 4 shows the decrease of the throughput with the operating time for various lifetime. Figure 5 shows the dependence of average throughput on the lifetime, where t_a is the active time defined in Fig.2 and the idle time t_i also defined in Fig.2 is assumed to be 15 min. When the lifetime is 10 hours, average throughput over 80% of the initial value can be attained by refilling every 4 hours. If the lifetime is longer than 20 hours, the same level of average throughput is possible by refilling every 12 hours.

4. Aligner

The overlay accuracy is required to be better than a quarter of the minimum linewidth. Major factors affecting the overlay are alignment error of the aligner, placement error of the mask pattern, and distortion of the wafer.

If it is assumed that the overlay is given by the root mean square of these factors and all the factors are the same, the error budget for each factor is about 14% of the minimum linewidth, that is 25 nm for the 180 nm feature size.

Many prototype aligners have been developed, several of which are listed in Tab.1. The principal objective of those aligners has so far been to achieve high alignment accuracy. Several research groups have demonstrated alignment

Fig.4 Decrease of throughput with operating time.

Fig.5 Dependence of average throughput on the lifetime of stored current.

accuracy better than 25 nm (3σ)[14-17].

As an example, experimental result of our laboratory is shown in Figure 6.

The alignment accuracy of aligner itself described above can meet the requirement for 1 Gb DRAM level. However, in application to device fabrication, overlay accuracy is significantly affected by errors caused by wafer processing and placement error of mask pattern[3, 18-20]. The former problem is not specific only to SRL but will be encountered by any advanced lithography. The issues related with masks will be discussed in the next section.

Fig.6 Experimental result of alignment repeatability.

From the viewpoint of production, development of high throughput aligners is strongly required. Recently, a few machines addressed to high throughput have been developed. One is being developed under the ARPA's program by SVGL, but reported to be behind the schedule. Another is XRS-2000 proposed by Karl Suss. The aligner developed by CANON is reported under evaluation experiments.

5. Mask

It is often said that mask fabrication is the bottleneck of SRL because of one to one printing. However, great progress has recently been made in this field. Table 3 shows requirements in mask fabrication of 180 nm feature sizes

Table 3 Status of X-ray mask measured with 1 Gb DRAM level (180 nm design rule)

Issue	Requirement	Present status
Resolution	<150 nm	>50 nm
Linewidth control	<15 nm (3σ)	16 nm (3σ)
Placement accuracy	<25 nm (3σ)	45 nm (3σ): EB writer placement Process-induced distortion 25 nm (3σ)
Radiation tolerance	> 10^6 shots	feasible with SiN, SiC, Diamond with optimized deposition condition
Defect inspection	>50 nm	feasible with inspection machine by KLA: SEMSpec
Defect repair	>50 nm	feasible with FIB application machine (MICRION, IBM)

and the present status. The remaining issue to be solved is improvement of the placement accuracy. The values for the placement accuracy shown in Tab.3 are those reported by Nash et al[20].

What is the most important is development of an EB writer optimized for X-ray mask fabrication. The best data of EB writer placement ever reported is sub-20-nm[21]. Moreover, the placement accuracy can be improved by about two times by making use of a multiple-exposure method[22]. Patterning on the X-ray absorber film of high atomic number is strongly affected by the electron proximity effect. To cope with this problem, the acceleration energy of EB should be higher than at least 50 keV[20, 23].

6. Extendibility

Figure 7 shows the wavelength dependence of the ultimate resolution of SRL, together with similar relationships for the optical stepper and the EUV projection lithography, for comparison[24,25]. It is indicated that the resolution of 100-50 nm can be attainable with the proximity gap of 15-5 micron at the wavelength around 0.7 nm. However, to establish a practicable technology for such a fine pattern replication, issues concerning mask fabrication, printing process, and aligner operation with the narrow proximity gap need to be solved.

Fig.7 Wavelength dependence of the ultimate resolution of SRL together with that of EUV projection lithography and optical stepper.

Fig.8 0.17 micron pattern
obtained with usual
rinse process.

Fig.9 0.1 micron pattern
obtained with improved
rinse process.

Difficulties in fabricating fine absorber patterns can be reduced by making use of phase shift effect of X-rays[26-28]. It has been shown that due to this effect, relatively thin absorber of 0.3-0.4 micron in thickness provides highest contrast[29].

One of issues in printing process is pattern collapse during development, as shown in Figure 8. This phenomenon is common to any other lithography and may become more and more serious with decrease in the feature size. It has been found that the force causing the collapse is the surface tension of the rinse liquid[30]. On this basis, several process techniques effective to eliminate the pattern collapse[31,32] have been developed. Figure 9 shows 0.1-micron pattern delineated with an improved process.

The narrow proximity gap is not taken to be compatible with fast motion of the wafer stepping stage, since the mask membrane deforms during relative motion of mask and wafer and recovers only slowly[33]. However, experiments and simulation results at our laboratory show possibility to manage this problem without serious effects. Detailed investigation is now in progress[34].

7. Summary

The present status of SRL and its possibility down to 0.1-micron features have been described. The key issues in 180 nm dimensional region are improvement of pattern placement accuracy of masks and development of high throughput aligners. In order to upgrade SRL to a production-viable level, it will be necessary to optimize the whole SRL system. From this point of view, throughput is a good measure, since almost all components of SRL system relate with it. Another important issue is further improvement of the reliability. The SRL system is considered to be cost-effective only when many aligners are operated with single SR source. Thus, extremely high reliability is required of the SR source. This can be accomplished by establishing proper maintenance schemes based on accumulated data on operation, maintenance, and troubles at existing SR facilities routinely operating.

Technical problems associated with fine pattern replication of order of 0.1 micron have been also discussed. The possible solutions presented will lead to the extendibility over several generations of ULSI.

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