MICROPATTERNING

FOR ADVANCED INTERCONNECTIONS

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Ultra-large integrated devices require an increase in density and number of interconnection levels. The design rules for 0.18 μm technologies are 0.2 μm for the holes and 0.3 μm lines and spaces patterns for the metal level. DUV lithography using advanced techniques will achieve such design rules. However, DUV materials based on chemical amplification have not yet reached full maturity. In this paper, we have investigated their ability to achieve advanced interconnections for both lithography and etching.

Regarding the lithographic performance, the two main problems to be overcome are the sensitivity to both delay time and substrate type. We propose a physico chemical method based on DSC measurements to screen the materials able to be processed with minimized sensitivity to both delay and substrates.

The selected materials, positive and negative tones, as well as optimized lithographic processes have been used to investigate their etching durability.

For the etching step, the main parameters to be considered are the resist selectivity to the etched layer and the resist mask integrity during etching. When using High Density Plasma for oxide etching, the resist mask is modified, leading to striations on the sidewalls of the holes which requires optimization for 0.2 μm critical dimensions. In the case of Aluminum etching, the selected DUV resist shows a reduced selectivity as well as a bad sidewall passivation by the polymers compared to I-line photoresists. This will be a limitation to the conventional metal architecture which will be accentuated with the use of copper. The invert metallization schemes are promising as they only require dielectric etching which is less sensitive to the resist process.

This work has been carried out within the GRESSI consortium between CEA-Leti and France Telecom-CNET

1. Introduction

Ultra-large integrated devices require an increase in density and number of interconnection levels. The design rules for 0.18 μm technologies are 0.2 μm for the holes and 0.3 μm lines and spaces patterns for the metal level. DUV lithography using advanced techniques can achieve such

design rules. However, DUV materials based on chemical amplification have not yet reached full maturity. The compromise between resolution and sensitivity to delay effects is still under improvement.

In previous work [1,2] we have shown that the reduction in or elimination of delay time effects observed in DUV positive resists, and responsible for linewidth variations, is obtained when the lithographic film is soft-baked at above the glass transition temperature of the bulk matrix (T_g). In addition, the resist material must not be thermally degraded in order to preserve its lithographic properties. When these two conditions are fulfilled, a process window for process optimization can be defined, but this process window does not systematically exist. Before starting any process optimization, the available DUV positive materials are compared in terms of process window capability as well as their resulting sensitivity to delay time effect. The compared performances of APEX-E and UVIII positive tone resists from Shipley have been studied.

Another effect observed in the DUV chemically amplified resists is their sensitivity to substrate [3], particularly to doped oxides and nitride compounds. In the case of negative DUV resists an undercut is observed on top of the TiN substrate. As for the positive tone materials, the effect of the physico-chemical properties of the resist controlled by the baking temperatures has been studied [4]. The correlation between the T_g of the SNR 200 resist from Shipley company and the observed undercut are demonstrated.

The selected materials, positive and negative tone resists, as well as optimized lithographic processes have been used to investigate the material etching durability. The resist mask modifications during oxide and Aluminum etching steps have been studied. These two etching processes have been evaluated in order to estimate the capability of DUV materials for 0.18 μm design rule interconnections.

2. Experimental

2.1 Physico-chemical characterization

Differential Scanning Calorimetry (DSC) was used to determine the glass transition temperatures (T_g) of the different DUV materials (both positive and negative tones). The DSC analysis was performed on a TA instruments 2000 thermal analyzer. The heating rate was held at 10°C/min. The measurement was taken on resist samples obtained after scraping spin-coated and soft-baked wafers.

2.2 Lithographic experiments

For the lithographic studies, the experiments were performed in a 200 mm DUV lithographic cell, including a TEL Mark 8 track and an ASM-L 5500/90 DUV stepper.

The following process conditions were used for the DUV positive tone UV III and negative tone SNR 200 resists from Shipley.

2.2.1 UVIII resist process

- HMDS priming : 150°C, 70 s
- UV III resist coating (0.61 μm thickness)
- Soft-Bake (SB): 135°C, 60 s
- DUV exposure : NA = 0.5, sigma = 0.63
- Post Exposure Bake (PEB): 135°C, 60 s
- Development : MF CD 26 (0.26 N), 60 s single puddle

2.2.2 SNR 200 resist process

- HMDS priming : 150°C, 70 s
- SNR 200 resist coating (1.2 μm thickness)
- Soft-Bake (SB) : 140°C, 60 s
- DUV exposure : NA = 0.5, sigma = 0.63
- Post Exposure Bake (PEB) : 124°C, 60 s
- Development : MF 319 CD-14 (0.14 N), 120 s double puddle

2.3 Etching experiments

In this study the dielectric layer was etched in an Inductively Coupled Plasma (ICP) reactor (HDP Centura Dielectric Etch) from Applied Materials.

A Transformed Coupled Plasma reactor type from LAM research (TCP 9600) was used to etch the metal layer after lithography.

For both lithography and etching experiments, Scanning Electron Microscope (SEM) analysis was used to characterize the critical dimensions (in-line Hitachi 7280) and morphological aspect on cross-sections (high voltage Hitachi 4100).

3. Lithographic materials and processes

The reduction in or elimination of delay time effects observed in DUV positive resists, responsible for linewidth variations, implies the elimination of a large amount of free volume generated during the spin-coating process. This condition is fulfilled when the lithographic film is soft-baked at above the T_g of the bulk matrix and reaches a maximum T_g value [1]. In addition, the resist material must not be thermally degraded in order to preserve its lithographic properties. When these two conditions are fulfilled, a window for process optimization can be defined but this process window does not systematically exist. In order to select DUV materials with a minimized delay time effect, the DSC measurements were used as a screening method.

3.1 Screening method for positive tone DUV material selection

Figs. 1 and 2 present the DSC thermograms of the APEX-E, a resist currently used in production, and the UV III resist recently available on the market. The thermograms were obtained after a Soft-Bake (SB) of 100°C for 60s on a hot plate. For the UV III resist, a T_g of 144°C can be easily detected. A large endothermic peak, attributed to the thermal deprotection with a maximum at 186°C is also recorded. The DSC thermogram of the APEX-E shows only an endothermic peak at 135°C related to the deprotection reaction, and no glass transition can be detected. For this material, this implies that the deprotection of the resist film occurs before reaching a maximum compaction

state of the film. Therefore, a significant amount of free volume is left in the resist film allowing easy diffusion of Photo Acid Generator (PAG) molecules and contaminants from the environment.

Fig. 1 DSC thermogram of the Shipley APEX-E DUV positive resist.

Fig. 2 DSC thermogram of the Shipley UVIII DUV positive resist.

We have reported in Figs. 4 and 5 the SEM pictures representing the effect of the delay time between exposure and Post Exposure Bake (PEB) for these two materials. In the case of the APEX-E resist, after a 20 min delay, we observed a T-top characteristic of a loss of PAG at the surface of the exposed areas. In contrast, 0.3 μm holes patterned with the UV III resist (Fig. 4) are not affected by a 30 min delay.

The behavior of these two resists is therefore shown to be in good agreement with the DSC characterization technique. Thus, the DSC method can be used to select the DUV materials with minimized delay sensitivity and to optimize their process conditions.

3.2 Application to the SNR 200 DUV negative resist

When DUV negative tone resists are used on top of TiN, an undercut is observed at the resist/TiN interface (Fig. 5). The undercut observed is generally explained as the result of hindered crosslinking due to the quenching of the Photo Acid Generator (PAG) at the interface, or to the diffusion of contaminant molecules from the substrate. Whatever the diffusion phenomenon involved, diffusion of small molecules is known to be extremely dependent on the free volume content of the layer.

In previous studies [1,2], we have demonstrated that diffusion is minimized when the resist film is baked at above the glass transition (T_g) of the bulk material. This allows the elimination of the free volume trapped during film spin-coating.

a) b)
Fig. 3 SEM picture of 0.35 μm L/S patterns - Shipley APEX-E resist :
a) without delay.
b) with a 20 min delay between exposure and PEB.

Fig. 4 SEM picture of 0.3 μm holes - Shipley UVIII resist :
a) without delay.
b) with a 30 min delay between exposure and PEB.

Fig. 5 Definition of undercut = $(CD_B - CD_I)/2$ in the case of an isolated resist line

Fig. 6 DSC thermogram of the Shipley SNR 200 DUV negative resist

Therefore, as already presented for positive resists, the DSC thermal analysis has been used to characterize the SNR 200 negative resist from Shipley, and thus to determine its glass transition temperature. A correlation between the undercut and the glass transition temperature has been established.

3.2.1 DSC analysis of the SNR 200 DUV negative resist

Fig. 6 presents the DSC thermogram of the SNR 200 DUV negative resist after a SB at 100°C for 60 s on a hot plate. A T_g value of 115°C can be measured. A large endothermic peak, attributed to the thermal crosslinking of the resist, with a maximum at 185°C is also recorded. Thus, a thermal process window exists for which the free volume generated by spin-coating can be eliminated. This is made possible by baking the film at above the T_g measured and below the onset temperature of the crosslinking reaction.

3.2.2 Influence of baking temperatures on undercut

The undercut versus SB and PEB temperatures has been experimentally studied using statistical experimental design [4] and the resulting modeling is presented in Fig. 7. The value of the undercut varies between 0 and 0.2 μm ; for values higher than 0.15 μm , the 0.4 μm resist patterns fall down.

Fig. 7 Undercut versus SB and PEB temperatures of the SNR 200 negative DUV resist

The effect of the SB conditions appears clearly : the undercut decreases when the SB temperature is increased. This result is illustrated in Figs. 8 and 9 on 0.4 μm isolated resist lines. For a low SB temperature (110°C), the measured undercut is 80 nm, whereas for high SB conditions (125°C), this value is reduced down to 10 nm.

Concerning the PEB step, the undercut increases with the PEB temperature. The effect becomes significant for PEB temperatures higher than 120°C. An interesting point to note is that for both SB and PEB temperatures, the same boundary at 120°C can be observed. These results are

consistent with a diffusion involved mechanism, and are correlated with the T_g value measured by DSC ; indeed, diffusion is limited for a densified film, i. e. baked at above its T_g (115°C). Diffusion is thermally enhanced during PEB for temperatures above T_g . Thus limited diffusion, and therefore minimized undercut, is obtained for the following bake conditions : $SB > T_g$ and $PEB < T_g$.

Fig. 8 SEM picture of 0.4 μm isolated line
SNR 200 negative DUV resist
SB = 110°C, 90 s - PEB = 105°C, 90 s
undercut = 80 nm

Fig. 9 SEM picture of 0.4 μm isolated line
SNR 200 negative DUV resist
SB = 125°C, 90 s - PEB = 105°C, 90 s
undercut = 10 nm

Regarding positive tone formulations, the diffusion mechanism is governed by the physico-chemical properties of the resist and can be controlled by the bake temperatures (SB and PEB). When thermal treatments are considered, the glass transition temperature (T_g) is an important internal reference temperature and should definitely be considered.

4. Etching requirements

In addition to lithography requirements, the resist patterns must withstand stringent etching processes. For interconnections, two different types of substrates are etched : dielectric oxide and metal. The UVIII DUV positive resist was used for contact and via levels, whereas the SNR 200 DUV negative was implemented for the metal levels. We have evaluated the influence the etching conditions on the resist mask durability.

Fig. 10-a
SEM picture of 0.3 hole after complete oxide etching and resist stripping
a) top view, b) tilted view

Fig. 10-b

4.1 Dielectric etching

A good example of dielectric etching is given by the results obtained for the via level. A 1.2 μm thick oxide layer, deposited using a HDP reactor over a TiN underlayer, was etched after DUV lithography using the UV III resist. The SEM pictures of a 0.3 μm hole after etching and resist stripping is shown in Figs. 10a and 10b for top view and tilted observation respectively.

Fig. 11 Cross-section SEM picture of 0.5 μm hole after 10 s oxide etching without resist stripping

We can observe striations on the sidewalls of the hole due to significant roughness on the resist surface. The roughness of the resist mask is transferred into the oxide (Fig. 11). The SEM picture presented in Fig. 11 was obtained after 10 seconds in a C_2F_6 plasma. The resist degradation under plasma exposure has already been studied using XPS analysis in the case of novolak polymers [5] in a microwave multipolar plasma using a distributed electron cyclotron resonance. XPS analysis has shown that this degradation can be described as a graphitization of the resist mask. This bulk degradation has been attributed to the synergistic effects of ion bombardment on the polymer layer : a mechanical effect induces the volatilization of the hydrogen and oxygen from the polymer, whereas a thermal effect, which induces self-diffusion of the polymer chains at above T_g , is responsible for the extension of the graphitization into the bulk. This self diffusion mechanism becomes significant for low molecular weight polymers such as photoresists used in resist formulations. A complete analysis of this phenomenon in the case of DUV resists is under progress.

These results show that the resist mask modification is sensitive to the etching conditions. If the present process etching conditions are used, the extent of the striations represents 21% of the critical dimensions (CD). Assuming the same behavior for 0.2 μm holes, this etching process requires optimization in order to be compatible with the 0.18 μm design rule technology.

4.2 Metal etching

The etching results obtained for a metal level are given below for a negative type DUV resist (Shipley SNR 200). Compared to a standard I-line resist, the behavior of the SNR 200 resist presents two main differences. First, the resist consumption is greater than that of an I-line resist. As an example, for a metal stack including TiN ARC 400 Å/ AlCu 8000 Å/Barrier TiN 900 Å, a 7000 Å resist thickness is required for the I-line version, whereas a thickness of 10000 Å is necessary for the SNR 200. Secondly, due to a bad sidewall passivation by the polymers formed during the etching step, a lateral erosion of Aluminum is obtained. This phenomenon is shown in Fig. 12 for 0.6 / 0.4 μm lines and spaces of a metal stack after etching. Under these etching conditions, the only way to overcome this problem, is to increase the resist thickness. However, as design rules are decreasing, a reduced thickness is required for a good lithographic performance.

Among the different etching parameters, the bottom electrode power is the one with the most influence on both resist erosion and sidewall passivation, and therefore has to be minimized. Under these conditions, sidewall passivation can be achieved with a 1.2 μm thick resist. The results obtained under these optimized conditions are shown in Fig. 13 for 0.4 / 0.4 μm lines and spaces of a metal 1 stack after etching and resist removal.

The resistivity of Aluminum is not be compatible with 0.18 μm design rules and has to be replaced by copper. Two different types of chemistry can be used to etch copper. Chlorine chemistry requires a high temperature (250°C) to eliminate by-products [5]. Such conditions are not compatible with standard resist masks, and a hard mask is therefore required. Furthermore, using this chemistry, the control of copper corrosion is the main concern [6]. With methane-based chemistry, a conventional resist mask can be used but the etch rate is too low [7]. The invert metallization technology is a possible way of overcoming this problem. As observed in Fig.14, no more metal etching is needed : trenches are patterned in the dielectric and filled with the metal which is polished by Chemical Mechanical Polishing (CMP).

Fig. 12 SEM picture for metal level etching
0.6 / 0.4 μm L/S - SNR 200 resist
but for I-line resist etching process conditions

Fig. 13 SEM picture for metal level etching
0.4 / 0.4 μm L/S -SNR 200 resist and
optimized DUV resist etching conditions

Fig.14 Invert metallization scheme

With this interconnection scheme (Fig. 14), the required resist thickness will not exceed 0.6 μm for the trench etching which is compatible with the required lithographic resolution (0.3 / 0.3 μm lines and spaces).

5. Conclusion

The micropatterning of advanced interconnections requires DUV resist formulations offering high resolution and process stability together with plasma durability.

A characterization technique based on DSC measurements can be used to select high performance positive and negative DUV formulations. In both cases, detrimental effects due to parasitic diffusion are shown to be controlled by the thermal properties of the resists, i. e. the glass transition temperature (T_g).

The resist plasma durability has been evaluated in regards to dielectric etching for positive tone materials and metal etching for negative tone materials. Their plasma behavior induces limitations for advanced interconnections, mainly for metal etching. Therefore, new architectures, such as invert metallization, have to be considered for 0.18 μm design rule technologies.

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