Bottom Contact Ambipolar SWNT-FET Devices Using Flattened Electrodes

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We fabricated individual single walled carbon nanotubes (SWNTs) field-effect transistor (FET) in sub-micrometer channel using flattened bottom contact electrodes. By using spin-coating deposition method, an array of SWNTs-FET devices can be fabricated simultaneously in one large substrate. We compared our flattened electrodes to the non-flattened electrodes SWNTs-FET devices. The number of SWNTs direct junctions drastically increase by using flattened electrodes, especially at channel length of 200 nm. In this channel length, the number of SWNTs direct junctions in flattened electrodes is approximately 2 times larger than that of non-flattened electrodes devices. All of our devices also show ambipolar FET characteristic under vacuum condition. Our flattened electrodes devices have better balance of $p$- and $n$-channel mobility compare to that of non-flattened electrodes devices. These results show the advantages of flattened electrodes for bottom contact SWNTs-FET devices.

1. **Introduction**

Currently, single walled carbon nanotubes (SWNTs) field effect transistor (FET) devices can be fabricated by either chemical vapor deposition (CVD) or solution casting. Comparing to the CVD-based SWNTs devices, SWNTs devices which are fabricated by solution casting has an advantage since the recent purification method to separate metallic and semiconducting SWNTs on a large scale were done in SWNTs solution. In the case of sensing devices, direct junction of SWNTs on the metal electrodes is favorable to eliminate ambiguous response of the sensor. For the short channel length devices, electrodes are patterned by using electron beam lithography (EBL). In the top contact devices, the SWNTs must be deposited before applying EBL process. So, there is a risk since the SWNTs can be damaged by direct electron irradiation. Furthermore, there are several steps following EBL process, such as, resist removal and cleaning procedure. In the case of using silicon wafer as substrate, a metal buffer layer must be deposited prior to designated metal deposition, i.e., Cr/Au or Ti/Au. Then the SWNTs will make contact to that of buffer layer, whereas every metal has its own work function which can provide different electrical characteristic in semiconducting SWNT-metal junction. Therefore, it is important to fabricate good SWNTs devices by using bottom contact technique even in the short channel region.

2. **Experimental Details**

Flattened electrodes devices were fabricated on 300 nm SiO$_2$ surface grown on heavily n-doped silicon substrate which act as gate electrodes. S/D electrodes were patterned by using EBL. Subsequently, reactive ion etching were performed to reduce SiO$_2$ thickness of the patterned area of the substrate so that the S/D electrodes can be embedded into the substrates. Then, 8 nm of Cr and 42 nm of Au were deposited by using electron beam deposition onto the substrates. After lift-off and cleaning process, we flattened the metal electrodes by using method which is described in the previous report. For comparison to our flattened electrode SWNT-FET devices, we also fabricated non-flattened electrodes devices by using the same fabrication method excluding reactive ion etching and flattening process. Average heights of flattened and non-flattened electrodes are approximately 4 and 42 nm, respectively.

Semiconducting SWNT were deposited using spin coating method. Arc-discharge SWNT (NanoIntegris Inc.) containing 99% semiconducting SWNT having an average diameter of 1.4 nm were dispersed in dimethylformamide (DMF). The concentration of the SWNTs is about 10 μg/ml. The substrate were cleaned by piranha solution and modified by 1% 3-aminopropyltriethoxysilane (APTES, Sigma-Aldrich) in toluene for 1 hour under N$_2$ atmosphere prior to SWNT deposition. Then, 100 μl of SWNT dispersion were dropped into the spinning substrates. In this way, alignment of the SWNT on the electrodes can be controlled by adjusting relative position of the electrodes to the rotational center of the spinning substrate. After SWNT deposition, the substrates were heated at 150 °C inside vacuum oven for 1 hour to remove residual solvent. The FET characteristics of all devices were measured using Keithley 4200SCS semiconductor parameter analyzer at room temperature in vacuum and/or open air conditions.

3. **Result**

Fig. 1 shows atomic force microscope (AFM), tapping mode, images of SWNT junctions between S/D electrodes at different channel length (0.2, 0.5, 1, and 10 μm). SWNTs could form network or junctions between S/D electrodes due to strong attractive interaction between APTES-modified SiO$_2$ surface and the SWNTs. In addition, drop casting of SWNTs solution on to the spinning APTES-modified SiO$_2$ substrates could separate semiconducting and metallic SWNTs which is favorable in our research. In the case of short channel length devices, SWNTs tend to make direct junctions between S/D electrodes which are shown in Fig. 1(a), (b), (c), (e), (f), and (g). While in the case of long channel length devices, 10 μm, the SWNTs form...
percolation network and there is no significant difference of SWNT network between flattened (Fig. 1(d)) and non-flattened (Fig. 1(h)) electrodes devices.

![Figure 1. AFM images of individual SWNT junctions between the electrodes at different channel length: (a) and (c) are 0.2 µm, (b) and (f) are 0.5 µm, (c) and (g) are 1 µm, and (d) and (h) are 10 µm. The channel width is 20 µm. Top and bottom images are flattened and non-flattened electrodes, respectively.](image)

Qualitatively, by observing AFM images in Fig. 1, larger number of SWNTs direct junctions are found in flattened electrodes devices. In order to make quantitative comparison between flattened and non-flattened electrodes devices, the number of SWNTs direct junctions between the S/D electrodes were counted by using AFM images which were taken prior to electrical characterization. Five AFM images, 2 x 2 µm area, which consist S/D electrodes were randomly taken at different location on the same sample. The number of SWNT direct junctions which were counted by using AFM images which were taken at different location on the same sample. The number of SWNT direct junctions per 2 µm channel width are tabulated in Table 1.

Table 1. Estimated number of SWNT direct junction per 2 µm channel width.

<table>
<thead>
<tr>
<th>Channel length</th>
<th>Flattened electrode</th>
<th>Non-flattened electrode</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 nm</td>
<td>3.8±1</td>
<td>1.8±1.5</td>
</tr>
<tr>
<td>500 nm</td>
<td>4.6±2</td>
<td>2.8±1</td>
</tr>
<tr>
<td>1000 nm</td>
<td>3.4±1.5</td>
<td>3±1</td>
</tr>
</tbody>
</table>

We measured FET characteristic of flattened and non-flattened electrodes SWNTs-FET devices in short and long channel length devices. All devices show ambipolar FET characteristic in vacuum condition, while only p-type for open-air condition due to the band-bending at the interface between SWNTs and gold electrodes in the presence of oxygen gas.

Generally, carrier mobilities decrease as the channel length decrease. FET carrier mobility in flattened electrodes devices are lower than in non-flattened electrodes devices. In the cases of 0.2 and 0.5 µm channel length devices, there are small difference of the p-channel carrier mobility between flattened and non-flattened electrodes devices. But n-channel carrier mobility in flattened electrodes are higher than that of non-flattened electrodes. While in the cases of 1 µm channel length devices, p- and n-channel carrier mobility of flattened electrodes devices are lower than that of non-flattened electrodes devices. However, the balance of carrier mobility between p- and n-channel in flattened electrodes devices are better than in that of non-flattened electrodes devices. We consider this is caused by the bending effect of the SWNTs in non-flattened electrodes devices since deformation of CNT can change its electronic properties.

Selective burning of metallic SWNTs significantly improve the on/off ratio. We performed burning process in open air condition since our SWNTs-FET devices show p-type FET behavior rather than ambipolar. In a successful burning, on/off ratio increased from 5 to 7x10^2 and 2 to 2x10^3 for p- and n-channel, respectively. However during burning process, some of the semiconducting SWNTs were also burned resulting significant decrease for approximately 2-order of magnitude in both p- and n-channel carrier mobility. In addition, the probability of successful burning process is only 40% (two out of five trials).

4. Summary

Our results show that the use of flattened electrodes devices increase the number of SWNTs direct junctions between S/D electrodes. Although the presence of metallic SWNTs becomes serious contaminant, we still can observed FET characteristic in all devices. FET carrier mobility in flattened electrodes are relatively lower than in that of non-flattened electrodes devices. However, balance of p- and n-channel carrier mobility in ambipolar FET devices are increase by using flattened electrodes devices.

References