Degradation and Improvement of Electrical Properties of (Ba, Sr)TiO₃ Thin Film Capacitors by Heating Process

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Because of the increased need for higher levels of integration of capacitors and piezoelectric generators, such as in energy harvesting devices, the dielectrics used in capacitors have changed from traditional materials to complex oxides. One important candidate material for future integrated capacitors is (Ba,Sr)TiO₃ (BST), because of its high dielectric and piezoelectric constants and its low leakage current. However, growth of BST films requires high temperatures of about 700°C, and the electrical properties of BST can be degraded by patterning processes. In the present study, BST thin films were deposited on sapphire and Pt/sapphire substrates using RF magnetron sputtering. Layered capacitors were then prepared using a metal mask method, and in-plane capacitors with interdigital electrodes were fabricated by lithography and wet etching. The electrical properties of the capacitors were evaluated, and defect energy levels were investigated using thermally stimulated current (TSC) measurements. The TSC results indicated the presence of three kinds of defects in the BST, with activation energies of 0.6, 0.7 and 0.8 eV. An annealing process was carried out in an attempt to remove damage caused by wet processing. This was found to reduce the dielectric loss, and the optimum annealing temperature was determined to be 200°C.

Key words: Tunable device, BST, Coplanar waveguide, Microwave, Thin films

1. INTRODUCTION

Barium strontium titanate (Ba, Sr)TiO₃ (BST) thin films have been intensively investigated because of their large dielectric constant at high frequencies, which makes them suitable for applications such as dynamic random access memories, and bypass capacitors in microwave monolithic integrated circuits [1-3]. Recently, the nonlinear nature of the BST dielectric constant has attracted attention for RF tunable capacitors. BST capacitors are expected to exhibit a high permittivity and a low dielectric loss at microwave frequencies. Because the operating frequency and bandwidth of microwave circuits using tunable capacitors can be dynamically changed, the number of wireless RF transceiver modules, and consequently the size of mobile devices, can be reduced. BST thin films for capacitors have been produced using various deposition methods and substrates [4-6]. In many studies, MgO and SrTiO₃ single-crystal substrates have been utilized because they allow the growth of high-quality BST(100) films. However, sapphire, glass and SiO₂/Si substrates offer advantages such as low cost and higher chemical stability. We previously investigated the microwave properties of BST(111) films fabricated on sapphire and Pt(111)/glass substrates [7,8]. However, there have been few studies on waveguide-type capacitors such as interdigital electrodes (IDEs) based on BST(111) films. However, it is known that degradation of the electrical properties can easily occur for IDE capacitors due to damage caused by the wet process used during

patterning.

In the present study, degradation of the electrical properties of BST(111) IDE capacitors deposited on sapphire is investigated. The dependence of the degradation on the fabrication conditions, particularly the post-patterning heat treatment, is discussed, and optimization of the fabrication process is considered.

2. EXPERIMENTAL

RF magnetron sputtering (SPF-210H, Anelva) was utilized to deposit (Ba_x, Sr_{1-x})TiO₃ films. The sputtering conditions are summarized at Table I. For these conditions, the Ba content *x* was determined to be 0.5 using X-ray fluorescence spectroscopy. The substrates were single-crystal α -Al₂O₃(0001) wafers. The epitaxial films had a (111) orientation, with BST [011] // α -Al₂O₃ [012]. The BST films were polycrystalline with an average grain size of approximately 100 nm [7,8].

To measure the in-plane electrical properties, IDEs made from Al were fabricated using vacuum evaporation and electron-beam patterning. The electrode spacing was 1.0 μ m, as shown in Fig. 1. After patterning, the specimens were subjected to an annealing process in a tube furnace at a temperature of 100 to 300°C for 1 hour in air. The IDE leakage current and capacitance were measured using an electrometer (6517A, Keithley) and an impedance analyzer (4194A, Agilent), respectively.

To perform measurements in the film thickness direction, circular Pt electrodes with diameters of 0.2

mm were formed on BST/Pt/ α -Al₂O₃ structures by sputtering and metal mask patterning. The degradation of the electrical properties was evaluated using thermally stimulated current (TSC) measurements [9].

Table I Sputtering conditions for BST deposition

Substrate	α-Al₂O₃ (0001)
Target	(Ba_{0.5}Sr_{0.5})TiO₃
RF power	100 W
Substrate Temp.	650 °C
Gas pressure	1 Pa
Gas	Ar:O₂ = 9:1 (2 sccm)
Depo. time	1.0 h (400 nm/h)

Fig. 1 Schematic of IDE fabricated on BST for electrical measurements

3. RESULTS AND DISCUSSION

3.1 Improvement of electrical properties by heat treatment

Fig. 2 Dependence of IDE leakage current on annealing temperature

The in-plane leakage current characteristics of the IDE capacitors were first measured, and the results are shown in Fig. 2 for different annealing temperatures. For the unannealed BST film, a current of more than 10^{-6} A/cm² at 60 kV/cm was observed, because of damage due to the patterning process. As seen in the figure, annealing causes a significant reduction in the leakage current. For an annealing temperature of 100°C, the reduction is about one order of magnitude, and for higher annealing temperatures, the reduction is slightly

less.

Fig. 3 C - V characteristics for unannealed IDE

Fig. 4 Loss tangent vs. voltage curve for unannealed IDE capacitor

The dielectric properties of the IDEs were next evaluated. Figures 3 and 4 show the influence of the DC bias voltage on the capacitance and loss tangent for an unannealed IDE capacitor. In the C - V characteristics shown in Fig. 3, a peak is present around 0 V, and the curve fluctuates in an irregular manner. Since even at its minimum, the loss tangent is 31.6%, such a BST capacitor could not be utilized for tunable devices.

Fig. 5 Dependence of C - V characteristics on annealing temperature for BST IDE capacitors

Figure 5 shows the dependence of the C - V characteristics on the annealing temperature. It can be seen that whereas the unannealed BST capacitor exhibits irregular characteristics, annealing causes the curves to become more stable. The instability may be caused by moisture absorbed during the wet process, in addition to crystal defects induced by the electron-beam lithography process [10]. It is clear from the figure that annealing can cause the electrical properties to recover.

Fig. 6 Loss tangent vs. voltage curves for BST IDE capacitors annealed at different temperatures

In Fig. 5, the lowest capacitance is obtained following annealing at 100°C, and then increases with annealing temperature. The capacitance of the IDEs may be affected by the presence of a dead layer and interfacial void. A low-permittivity dead layer may form at the surface of the imperfect BST crystal during sputtering [11]. In addition, voids may exist at the interface between the Al and BST due to poor adhesion during the Al evaporation process [12]. It is thought that annealing at temperatures higher than 100°C causes a reduction in the thickness of the dead layer, and improves Al adhesion, thus causing the capacitance to increase as shown in Fig. 5.

As shown in Fig. 6, annealing also led to an improvement in the loss tangent. The dielectric loss decreased to 0.9% at 200°C, but then increased sharply at 300°C. This may be due to the fact that the chemical reactivity of Al increases considerably at higher temperatures, leading to damage at the Al/BST interface. From these results, the optimum annealing temperature is 200°C.

3.2 Analysis of electrical degradation

Based on the results of the electrical measurements, degradation occurred in the sputtered BST films because of the presence of crystal defects. However, analysis of defects in electronic ceramics is difficult using conventional techniques such as X-ray diffraction or electron microscopy. For analysis of defects in semiconductors and organic materials, TSC measurements have proved to be useful.

In TSC, a specimen on a heating stage is connected to an electrometer and a voltage source. It is subjected to pre-heating and is then cooled using an electric field in order to inject charge carriers into traps associated with crystal defects. The voltage during field cooling is called the trapping voltage V_t . Next, the specimen is heated slowly so that the trapped carriers are released. In order to collect the released carriers, the heated specimen is also subjected to a very weak electric field V_c . The very slight flow of released carriers is observed as a current using the electrometer. From the dependence of the current on temperature, the defect density and the activation energy for the traps can be evaluated using the following equation [13]:

$$I_{TSC} = I_0 \exp \left[-\frac{E_t}{kT} - \frac{\nu}{\beta} \int_{T_0}^T \exp \left(-\frac{E_t}{kT} \right) dT \right], \quad (1)$$

where E_t is the activation energy, ν is the escape frequency, and β is the heating rate. Since the equation contains nonlinear and integral functions, numerical integration and nonlinear fitting are used to solve for the density and the activation energy [14].

For TSC measurements on ferroelectric and high dielectric constant films, the measured current contains components peculiar to electronic ceramics, such as leakage and pyroelectric currents. Since it is necessary to reject redundant currents, a modified TSC process was used in the present study [9]. In this process, the carrier collection phase was carried out twice, and the cooling and heating rates were fixed. Measurement parameters such as the temperature and voltage were optimized, and the true carrier current from the traps was calculated using currents obtained during heating and cooling in the first and second phases [15].

Fig. 7 Dependence of TSC on (positive) trapping voltage

Fig. 8 Dependence of TSC on (negative) trapping voltage

The TSC measurements were carried out on Pt/BST/Pt multi-layered specimens, using V_c and β values of 5 mV and 2 K/min, respectively, which were found to be optimal for acquiring a clear signal. The dependence of the TSC signal on the trapping voltage was also evaluated. The results for positive and negative trapping voltages are shown in Fig. 7 and 8, respectively. The polarity was determined by the bottom electrode, with the top electrode being set to ground.

In Fig. 7, two TSC peaks at 130 and 180°C can be seen for a positive trapping voltage. The noisy signal observed for temperatures above 230°C is the result of the large leakage current, which increases rapidly at high temperatures. For a negative trapping voltage, there are also two peaks, although their peak positions are 180 and 210°C, as shown in Fig. 8.

Since the trapping voltage affects the injection efficiency for different types of defects, the voltage

dependence of each TSC peak differs. In particular, the TSC signal from defects at the interface is influenced by the voltage polarization, because electrons are injected into the top and bottom interfaces of the BST layer under a positive and negative voltage, respectively [16]. Thus, the peaks at 130 and 210°C that depend on the polarization are related to defects at the interface, whereas the peak at 180°C obtained for both polarizations is due to defects distributed throughout the film, such as grain boundaries in the columnar structure produced by sputtering deposition. The activation energies for the peaks at 130, 180 and 210°C were calculated to be 0.7, 0.6 and 0.8 eV, respectively, using Eq. (1). The electrical properties of the IDE capacitors are also expected to be degraded by these three types of defects. However, because the density and activation energy of defects at the bottom interface may be influenced by the Pt bottom layer, a detailed investigation of the dependence of the TSC peaks at 130 and 210°C on the interfacial conditions is required [9]. Clarifying the actual nature of the crystal defects and the mechanism by which they degrade the electrical properties is a topic for future work, and will require the combined use of TSC and other physical evaluation methods.

4. CONCLUSIONS

In order to investigate the feasibility of BST films in coplanar-type device applications, their in-plane electrical properties were evaluated using IDE capacitors with a 1-μm electrode spacing. A remarkable degradation of the electrical properties was indicated by leakage current and capacitance measurements, and was attributed to damage induced during the fabrication process. A post-patterning heat treatment was found to be effective at recovering the electrical properties, with the optimum temperature being 200°C. The loss tangent decreased from 31.6% to 0.9% under these conditions. However, too high a temperature, such as 300°C, caused the electrical properties to become worse. The results of a TSC analysis indicated that there are three kinds of traps in the BST film, with activation energies of 0.6, 0.7 and 0.8 eV. The trap at 0.6 eV was related to bulk defects such as grain boundaries, whereas the others were due to interface defects. Additional investigations should be carried out into the degradation mechanism in order to further improve the electrical properties.

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