Mobility Behavior of Polycrystalline $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ Grown on Insulators

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We have examined the formation of the undoped polycrystalline $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ (poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$) layers grown on SiO_2 by using the solid phase crystallization method. We have investigated the electrical property of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers with the Hall effect measurement. We clarified the effects of the Sn incorporation into $\text{Si}_{1-x}\text{Ge}_x$ and the two-step solid phase crystallization on the Hall mobility. We found that the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers are crystallized over 475 °C-annealing. No Sn precipitation is observed after the crystallization of the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer with a Sn content of 1.3%. We can see that a large grain size can be achieved with the lower annealing temperature for $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ with a lower content of Sn. On the other hand, a higher mobility is obtained with the higher annealing temperature for the sample at a Sn content of 1.3%. We performed the additional 2nd-step annealing at 700°C for 10 min, and the mobility was effectively improved to be 1.5 times higher (129 $\text{cm}^2/\text{V}\cdot\text{s}$) than that before the 2nd-step annealing.

Key words: silicon, germanium, tin, polycrystal, mobility

1. Introduction

The monolithic three-dimensional (3D) integrated ultra large-scale integrated circuits (ULSI) technology is much attention for improving in the integration degree and realizing multi-functional devices with nanoelectronics and optoelectronics. The formation of polycrystal semiconductor thin films on insulator is an attractive candidate for the fabrication of stacking structures alternative to wafer bonding and through-silicon-via technologies. Considering the high speed driving of transistors, polycrystalline thin films with a high crystallinity is required for 3D ULSI applications. Also, a low temperature process of polycrystalline layers is needed to keep compatibility with metal contacts and interconnects in underlayers [1]. In addition, low off-leak current in transistors is necessary for low power consumption.

Polycrystalline- $\text{Si}_{1-x}\text{Ge}_x$ (poly- $\text{Si}_{1-x}\text{Ge}_x$) is an attractive candidate material for realizing requirements mentioned above. The energy band gap of poly- $\text{Si}_{1-x}\text{Ge}_x$ with a Si content as high as 20% is as large as 1 eV, which is comparable to bulk Si, hence the sufficient off-leakage current can be expected in the poly- $\text{Si}_{1-x}\text{Ge}_x$ metal-oxide-semiconductor field effect transistor.

The formation of poly- $\text{Si}_{1-x}\text{Ge}_x$ layer by using the solid phase crystallization (SPC) from amorphous phase has been reported [2-4]. However, the crystallization temperature of poly- $\text{Si}_{1-x}\text{Ge}_x$ is generally as high as 550-700°C [2], and such high crystallization temperature is not suitable for the fabrication process of 3D ULSI devices.

Previous works have been reported in which the crystallization temperature of amorphous-Si (a-Si) and a- $\text{Si}_{1-x}\text{Ge}_x$ to polycrystal phase can be reduced by the metal

introduce crystallization (MIC) process using Ni and Al [5-8]. However, there is a concern that these metal atoms remaining in polycrystalline layer become contamination forming deep-level defects.

Here, we are focusing on the incorporation of Sn into a- $\text{Si}_{1-x}\text{Ge}_x$ to reduce the crystallization temperature, because the incorporation of Sn promises to prompt the crystallization due to the low eutectic temperatures of Si-Sn and Ge-Sn binary alloys (~231 °C). Also, Sn would be familiar for Si and Ge LSI technology as polycrystallization catalyst compared to group-III or V dopant elements or metal impurities, since Sn is a group-IV element and Sn atoms are incorporated into the substitutional site in the diamond structure of $\text{Si}_{1-x}\text{Ge}_x$.

In addition, some papers reported $\text{Ge}_{1-x}\text{Sn}_x$ polycrystallization at a low temperature [9-11]. We recently reported the formation of poly- $\text{Ge}_{1-x}\text{Sn}_x$ layer by the liquid-Sn-driven lateral crystallization process with low temperature annealing at 240 °C for a-Ge layer [9]. We also reported that poly- $\text{Ge}_{1-x}\text{Sn}_x$ layer can be grown on an insulator film by using the SPC [11]. We found the advantage that the Sn incorporation into a-Ge reduces the crystallization temperature from 450°C to 430°C for 5 h-annealing, enhances the grain size of the polycrystalline layer, and improves in the hole mobility from 20 to 100 $\text{cm}^2/\text{V}\cdot\text{s}$ [11].

Moreover, $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ is an attractive material for optoelectronic applications such as solar cell and quantum well laser [12-14]. On the other hand, a problem is the Sn precipitation during the polycrystallization of $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ due to the low thermal equilibrium solid solubility limit of Sn in Si or Ge, (0.1 at.% in bulk Si, and 1.0 at.% in bulk Ge) [15, 16]. Recently, we reported the

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effect of the Sn incorporation into poly- $\text{Si}_{1-x}\text{Ge}_x$ [17]. The advantage of Sn incorporation is the increase in the crystallization velocity, the enhancement of the grain size, and the improvement in the hole mobility compared to polycrystalline without Sn. However, in our previous report, the mobility of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ was lower than that of poly-Si. Also, the electrical property of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ has not yet been clarified in detail. In this study, we clarified the electrical conduction mechanism in poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer in order to improve in the mobility.

2. Experimental procedure

N-type Si(001) wafers covered with a 1- μm -thick SiO_2 layer were used as substrate. A 120-nm-thick amorphous $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer was deposited at room temperature by using a molecular beam epitaxy (MBE) system. The base pressure of the vacuum chamber was below 7×10^{-8} Pa. Ge and Sn were deposited with Knudsen cells and Si was deposited with electron-gun evaporation. The target ratio of Si to Ge of $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ was designed as 1 to 3. The contents of Si, Ge, and Sn in amorphous $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ are shown in Table I. The contents of Si, Ge and Sn were estimated by using Auger electron spectroscopy (AES). The Sn contents for prepared samples were 0%, 1.0%, 1.3%, 3.0%, and 6.8%. Then, after cleaning the surface of $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ with dilute HF for 30 sec, an 15 nm-thick SiO_2 cap layer was deposited at room temperature. Finally, samples were annealed at 475–700°C for 5–15 h in N_2 ambient for the polycrystallization.

Table I: Si, Ge, and Sn contents in samples.

Sample#	Si content (%)	Ge content (%)	Sn content (%)
1	23.0	77.0	0
2	32.3	66.7	1.0
3	29.0	69.7	1.3
4	16.7	76.5	6.8

The crystal structure was characterized by using X-ray diffraction (XRD). The electrical property was investigated by using the Hall effect measurement system with the van der Pauw method.

3. Results and discussion

Figure 1 shows the grazing angle XRD profiles for samples with a Sn content of 1.3% after annealing at 450, 475, and 500 °C for 5–15 h. The X-ray source used was the Cu-K α line with a wavelength of 0.154056 nm. The incident angle of X-ray to the sample surface was 2.823°, and we can see the strong peak of the Si311 Bragg reflection at a diffraction angle of 56.115°. No peak of the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ Bragg reflection is observed before and after annealing at 450–475 °C for 5 h. However, we can see some clear diffraction peaks of the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer with annealing at 475 °C for 15 h and at 500 °C for 5 h. Those peaks are related to Bragg reflections similar to $\text{Si}_{1-x}\text{Ge}_x$ 111, 220, and 311. This result means that amorphous- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ can be crystallized with

annealing over 475 °C.

No diffraction peak of β -Sn is observed at a Sn content of 1.3%, which means no Sn precipitation. On the other hand, in the sample with a Sn content as high as 6.8%, Sn precipitation is observed after annealing (*not shown*).

Fig.1: Grazing angle XRD profiles for $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ with a Sn content of 1.3% after annealing.

Then, we estimated the grain size of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers from the full width half maximum (FWHM) of these diffraction peaks by using the Scherrer's equation as follows,

$$D = \frac{0.9 \lambda}{B \cos \theta} \quad (1)$$

where D is the grain size, λ is the wavelength of X-ray, B is the FWHM value of the diffraction peak, and θ is the Bragg angle. Figure 2 shows the annealing temperature dependence of the grain size of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers with a Sn content of 0% to 6.8% after 5 h or 15 h annealing. The grain size is averaged by it derived from Bragg angles of 111, 220, and 311 reflections. We can see that a large grain size can be achieved by the introduction of Sn. Especially, a lower Sn content is effective to obtain a larger grain size. Also, a higher grain size is obtained with a lower annealing temperature at a lower Sn content. However, in the case of a Sn content of 6.8%, the grain size decreases with the annealing temperature. These results suggest that the nucleation density of polycrystal grains can be suppressed by lowering the Sn content and the annealing temperature.

Next, we investigated the electrical property of the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers. We estimated the carrier mobility and the hole concentration of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers by using the Hall effect measurement system. Figure 3 shows the carrier concentration dependence of the Hall hole mobility of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers. The mobility of single crystal Si is also shown for comparison [18]. From the Hall effect measurement result, p-type conduction is observed for all $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ samples even though the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers were undoped. This is considered that the point defects related to vacancy play a role of acceptor in poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers [19]. Without Sn, the Hall hole mobility of poly- $\text{Si}_{1-x}\text{Ge}_x$ is around 40 cm^2/Vs . Hellberg *et al.* reported that mobility of poly- $\text{Si}_{0.2}\text{Ge}_{0.8}$ crystallized

Fig.2: The annealing temperature dependence of the average grain size of poly-Si_{1-x-y}Ge_xSn_y layers with n Sn content of 0% to 6.8% after 5 h- or 15 h- annealing.

by 650°C annealing is about 30 cm²/Vs [20]. So, we attain higher mobility than past report. The mobility increases with decreasing in the carrier concentration. Also, the mobility of the Si_{1-x-y}Ge_xSn_y layer with an Sn content of 1.3 % is half as high as that of single crystalline Si. We can see the introduction of a low content Sn of 1.3% effectively decreases the carrier concentration, and improves on the mobility of poly-Si_{1-x-y}Ge_xSn_y.

Fig.3: The Hall hole concentration dependence of the Hall mobility for Si_{1-x-y}Ge_xSn_y layers with the Sn content of 0 to 6.8%.

Therefore, we focus on the electronic properties of the Si_{1-x-y}Ge_xSn_y with a Sn content of 1.3% in detail. Figure 4 shows the annealing temperature dependence of the mobility and the carrier concentration for Si_{1-x-y}Ge_xSn_y with a Sn content of 1.3%. We can see that a higher mobility and a lower carrier concentration are obtained with a higher annealing temperature. However, we need the low temperature process for 3D integrated device as explained in the introduction. Toko *et al.* reported that the 2nd step high temperature and short time annealing after the low temperature polycrystallization of Ge is effective to improve on the mobility because low and high temperature annealing are effective to the increase of grain size and reduction of the carrier concentration

respectively [21]. Therefore, we examined the 2nd step annealing for the Si_{1-x-y}Ge_xSn_y sample with low temperature crystallization in order to improve on the mobility. We performed the additional 2nd step annealing at 700 °C for 10 min for the sample with an Sn content of 1.3 % after 1st-step annealing at 475 °C. As a result, the mobility was effectively improved to be 1.5 times higher and carrier concentration is less than before 2nd annealing. Moreover, this mobility is higher than that of the sample after annealing at 700 °C for 5 h.

Fig.4: The annealing temperature dependence of the Hall hole mobility for the Si_{1-x-y}Ge_xSn_y layer with an Sn content of 1.3%.

Next, we estimated the temperature dependence of the electrical property of these Si_{1-x-y}Ge_xSn_y layers to investigate the reason why the mobility is improved by the 2nd step annealing. The Seto model has been proposed to explain the electrical conduction mechanism in a polycrystalline semiconductor thin film [18]. In the Seto model, a grain boundary potential is formed with these grain boundary traps. The carrier mobility of the polycrystal semiconductor is represented by the equation as follows,

$$\mu = Lq \left(\frac{1}{2\pi m^* k_B T} \right)^{1/2} \exp \left(-\frac{E_B}{k_B T} \right) \quad (2)$$

where μ is the mobility, L is the grain size, E_B is the grain boundary potential, T is the temperature, k_B is the Boltzmann constant, m^* is the effective mass of hole of germanium, and q is the elementary charge.

Figure 5 shows the Arrhenius plot of the mobility of the poly-Si_{1-x-y}Ge_xSn_y layer with a Sn content of 1.3% after the 1st and 2nd step-annealing. We can see linear region for both plots. Considering the Seto model, we can estimate the grain boundary potential from the gradient of the linear region. As a result, the grain boundary potentials are estimated to be 17 and 11 meV for each sample as shown in Fig. 5. These values are less than a $k_B T$ value of 26 meV at 300 K. So the effect of the grain boundary potential on the carrier mobility seems to be negligibly small. Considering the sample after the 2nd annealing, the Arrhenius plot of the mobility does not shows a linear relationship near room temperature (more than 172 K). This result suggests that carrier scattering dominantly occurs not at the grain boundary but in the grain. This result suggests that the 2nd step annealing decreases the defect at the grain. As a result, it is

Fig.5: The Arrhenius plot of the mobility for the poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer with an Sn content of 1.3%.

suggested that the reduction of the defect at the grain and the increase of grain size lead to the improvement on the mobility.

4. Conclusions

We investigated the effect of the Sn incorporation and the annealing on the crystalline structure and the electrical property of the poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layers on insulator. A larger grain size can be achieved by a lower temperature annealing at 475°C for the $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer with a low Sn content of 1.3%. The introduction of a low Sn content of 1.3% into $\text{Si}_{1-x}\text{Ge}_x$ layer effectively improves on the mobility. We found that a higher mobility is obtained with a higher annealing temperature. We demonstrated that the mobility of poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer with a Sn content of 1.3% is improved by the two-step annealing owing to the increase of grain size and the decrease in the grain defect. The high mobility poly- $\text{Si}_{1-x-y}\text{Ge}_x\text{Sn}_y$ layer promises to be a candidate semiconductor material for future 3D LSIs.

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6. References

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