The Design Challenges of IoT: From System Technologies to Ultra-Low Power Circuits

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SUMMARY In order to realize an Internet-of-Things (IoT) with tiny sensors integrated in our buildings, our clothing, and the public spaces, battery lifetime and battery size remain major challenges. Power reduction in IoT sensor nodes is determined by both sleep mode as well as active mode contributions. A power state machine, at the system level, is the key to achieve ultra-low average power consumption by alternating the system between active and sleep modes efficiently. While, power consumption in the active mode remains dominant, other power contributions like for time-keeping in standby and sleep conditions are becoming important as well. For example, non-conventional critical blocks, such as crystal oscillator (XO) and resistor-capacitor oscillator (RCO) become more crucial during the design phase. Apart from power reduction, low-voltage operation will further extend the battery life. A 2.4GHz multi-standard radio is presented, as a test case, with an average power consumption in the μ W range, and state-of-the-art performance across a voltage supply range from 1.2V to 0.9V.

key words: wireless transceiver, sleep mode, ultra-low-power

1. Introduction

While Moore's law has been supporting miniaturization, power reduction and cost savings for many decades, the new IoT applications put unprecedented challenges on cost and battery size for IoT sensor node end points. These end points will become –invisibly– integrated in our smart buildings to monitor and adapt lighting, access, location based services, etc. For personal health care, wearable sensor nodes need to be lightweight and flexible, operating from small, printed batteries. For both applications, apart from many practical challenges on standardization, maintenance, etc., power consumption remains the root bottle neck for implementing this vision on an ubiquitous IoT.

2. Transforming Economy and Society

From a societal angle, we are undergoing the largest and fastest period of transformations in human history. Urbanisation is happening at an unprecedented speed in parts of Asia-Pacific, and worldwide, the urban population is estimated to double by 2050. This puts enormous pressure on strained resources like water, energy, clean air, and the management of this vast urban regions, in terms of logistics, mobility and sustainability, has become hugely complex. His-

torically the operation of assets like public transport and roads, hospitals, water, energy, a.o. has been inefficient. For example, London loses almost 25% of its fresh water every day through cracked and leaking pipes, this corresponds to a loss of water for 2M people/day.

In manufacturing, mass-customization is happening and goods are tailored to individuals. Logistics companies are advertising and delivering their goods on the right spot, at the right moment with an unprecedented granularisation. “Companies” like AirBnB and Uber build on shared creation, production distribution and consumption of goods and services. This is giving rise to a “sharing economy” where consumers have become users rather than owners of the goods. Our offices are becoming flexible, with a guaranteed service level in terms of ICT, cleaning or facilities; and a predictable energy consumption.

These megatrends are summarized in and [1], as presented by Accenture at the World Economic Forum in 2015. In the past century, we have moved from efficient manufacturing, to a service focused economy. Currently, we are transitioning into the era of an “Outcome based economy” where companies sell a measurable outcome, in terms of “flight hours” on a Boeing plane, “pay-per-lux” on a Philips lighting installation, etc. In a next wave, the “Autonomous Pull” economy, will become enabled by technologies for real-time demand sensing, as well as advanced cyber-physical interactions where machines and people interact and collaborate for a pervasive transformation of economy and society.

These deep transformations rely on the ability to gather a massive amount of data, and are fundamentally enabled by billions of sensors in a hyper-connected world. This is

Fig. 1 The adoption and impact path of IoT [1]

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what we have come to know as the Internet-of-Things. In this paper, we will focus on the end-points of IoT, and more specifically, on the ultra-low power connectivity as needed for these end points to become invisibly embedded in our smart environments.

3. IoT System and Circuit Design Challenges

As this paper focuses on the IoT end points, it is good to understand the broad and varied range of challenges on these nodes, from a system point-of-view. This section shows the analysis, starting from a generic IoT network, of important parameters/aspects need to be taken care of when designing the IoT end points.

Figure 2 shows a generic end-to-end solution, which consists of leaf nodes of sensor network, router nodes, a gateway and finally the Cloud where sensor data is stored and processed real-time.

3.1 Power and Performances

The scale of the platform is determined by the number of the end nodes. Therefore, the performance, the lifetime, the maintenance and the cost of each node are crucial to keep the system running efficiently. For wireless communication, the most important performance is link budget margin, which is defined by transmitter power and receiver sensitivity. The power consumption of the node needs to be minimized to extend the battery life, thus to reduce the frequency of the battery replacement, which is part of the maintenance. Cost can be reduced by highly integration, in terms of functionality: radio, memory and sensor; also in terms of off-chip components, and the silicon area. Such highly integration also leads to small form factor, which is especially essential for wearables.

3.2 Standards Compliance

Apart from the physical requirements, spectrum, as a scarce resource, adds another dimension of requirement. The 2.4GHz ISM band is crowded with multiple WiFi flavors, Bluetooth and ZigBee. While subGHz band is seeing new standards, like LoRa, SigFox and NB-IoT, as shown in

Fig. 2 Generic IoT platform

Fig. 3. All these standards need to co-exist and need orchestration in order to guarantee Quality-of-Service. From a HW perspective, this situation calls for multi-standard radio ICs, with limited area or bill-of-material overhead. It needs a revival of approaches similar to former “SW-defined radios”, with a single RF architectures that can support multiple standards. These new reconfigurable architectures do need to live up to the promise of very limited cost and power overhead as compared to single-standard solutions.

3.3 Security Consideration

Last but not least, security and privacy are considered the weakest link of IoT. As the end points are optimized for cost and battery life, often security comes as an afterthought and recent security attacks like [2] demonstrate how IP camera’s and other IoT endpoints are becoming maliciously used to create outages and congestion on the internet. Traditional mechanisms for secure booth, encryption a.o. are often not suited for the resource constrained end-points. Hence, there is a need for innovative low-cost and low power mechanisms for lightweight security for end-points. Apart from the optimization of keys and encryption algorithms, also new mechanisms can be used. As an example, a secure sensor location or a securely determined proximity between people and/or devices can be used as an additional authentication factor for the IoT end point. Today such feature, is already a key differentiator for NFC solutions where the physical limitation on distance provides a level of security and privacy. If based on secure propagation parameters, these ideas can be expanded to RF-based distance estimates. Further analysis goes beyond the scope of this paper.

Fig. 3 IoT application scenario with different standards

3.4 Short-Range Radio Design Considerations and Challenges

The system specifications and requirements in the end are translated into circuit design specifications. In this paper we focus on 2.4GHz short-range radios which target at indoor smart building systems and wearable devices. For such applications, power consumption and form factor are the key parameter to be optimized, with the goal of extending battery life, and being integrated and worn invisibly. Circuit implementation and smart power management are the two aspects to achieve power optimization. To reduce form factor, higher-level integration of RF matching network, antenna switch and any possible filters is necessary, without degrading the performance. Therefore, transmitter efficiency, receiver noise figure and linearity need to be take extra care. A 2.4GHz radio is presented in the following section, to show how to accommodate the above mentioned requirements, from circuit level, to achieve ultra-low power consumption, small form factor and state-of-the-art performance.

4. Case Study: An Ultra-Low Power Multi-Standard (BLE/IEEE802.15.4) IoT Transceiver SoC Optimized for Battery Life

The 2.4GHz radio SoC, proposed as the case study, complies with several short range standards, including Bluetooth low energy 4.0/4.2/5.0PHY, 802.15.4 and a 4Mbps proprietary mode. The measured receiver sensitivity for BLE 4.0 is -93dBm and maximum output power is 1dBm . The radio consumes 5.6mW in active receiving mode and 8.4mW in transmitting mode (with 0dBm output power), from 1V power supply. The circuit level sleep mode power consumption is $1.5\mu\text{W}$ from 1V .

To maximize battery life, a two-phase supply scheme is defined, as shown in Fig. 4. During phase I, the end node is supplied by the battery through an low dropout (LDO) regulator, which provides stable power supply as comparing to switching regulator. The voltage drop across the LDO is 200mV , therefore, the 1-V end node stops working when the battery voltage drops to 1.2V . However, for a low cost alkaline battery, the life time from 1.2V to 0.8V accounts

Fig. 4 Supply scenario w/o LDO

up to 60% of the total life time [3]. In order to make full use of the extra 60% of time, a phase II is proposed. During phase II, the end node is directly attached to the battery, saving the 200mV voltage drop, and extending the battery life. In phase I, sleep mode power consumption can reach nW -range, by switching off the LDO. While in phase II, as LDO is bypassed, sleep mode power consumption is dominated by circuit level leakage. In order to minimize the average power consumption, sleep mode power consumption of the radio needs to be minimized.

The block diagram of the proposed SoC is shown in Fig. 5, including analog front end, complete digital base-band, a MCU core and SRAM. Small form factor and low cost are guaranteed by only one external component, i.e., XO, since on-chip matching network and antenna switch are integrated. The architecture choice of the analog front end features a sliding-IF receiver and a 2-point polar transmitter, both of which are energy efficient. RX benefits from the LO planning: 1.92GHz ($4/5$ LO) for first RF mixer and 480MHz IQ signal for second mixer. TX achieves high energy efficiency by removing conventional IQ up-converter and implementing high efficiency Class-D PA. The all-digital phase locked loop (ADPLL) supports both TX and RX, offering a frequency range from 1.9GHz to 2.4GHz . The inductor in LC-tank based digitally controlled oscillator (DCO) has maximum Q at 2.4GHz to improve the TX efficiency. Further energy-saving is accomplished by system-level optimization, taking full advantage of the duty-cycled nature of IoT application.

4.1 System Level Optimization

Even with the state-of-the-art mW -range radios [5]–[10] a coin-size 150mA-Hour battery can only last hundreds of hours. Thanks to the duty-cycled nature, most of the IoT end points spend much longer time sleeping, instead of actively sending or receiving, leading to a μW -range average power consumption. Figure 6 shows the operation modes of a typical IoT node: active sending/receiving modes and sleep modes. For more and more applications, such as smart

Fig. 5 Block diagram of the 2.4GHz multi-standard compliant transceiver [4] (©2016 IEEE)

Fig. 6 Power modes of a generic IoT node over time

Fig. 7 Description of clock activity in (a) low duty-cycle case; (b) high duty-cycle case

building, industry monitoring etc, sleep mode power consumption dominates total average power, thus attracts the primary optimization effort.

4.2 Sleep Mode Power Optimization

Circuit blocks running during sleep mode include a system clock, a power state machine and a retention memory, to tracking timing for next event, to switch on/off circuits, and to keep necessary information when the radio wakes up. Power optimization is thus based on those three aspects. First, for the system clock, reusing crystal oscillator is an effortless option at the expenses of high power consumption. In the proposed work, XO consumes $180\mu\text{W}$, leading to the averaged power toward $200\mu\text{W}$, which is more feasible for wearable nodes, or data-streaming devices with rechargeable batteries, as shown in Fig. 7 (a). An alternative is to adopt a 200nW RC oscillator (RCO) as the system clock and implement a deep sleep mode. Waking up from deep sleep, XO need to be switched on first and the system enters sleep mode. Once XO is stable, the system enters active mode as sketched in Fig. 7 (b).

Timing overhead translates into power overhead in a duty-cycled system, therefore set a requirement on RCO accuracy and calibration time. Taking an example of $500\mu\text{s}/5\text{s}$

Table 1 Power states definition

Clock	Power domain	Deep sleep	Sleep	Standby	TX	RX
RCO	Always-on	On	On	On	On	On
XO	MCU	Off	On	On	On	On
XO	DBB ctrl	Off	Off	On	On	On
XO	DBB+AFE	Off	Off	On	On	On

duty ratio and considering the 32kHz RCO, an accuracy of 0.01% introduces an error of one packet time, meaning the active power consumption is doubled. Further degrading the accuracy causes more power overhead. Therefore, in the proposed work, the target accuracy of the RCO is set to 0.01% , and achieved by calibration using the 32MHz XO clock. A counter-based calibration scheme is implemented, by counting the number of XO clocks within a certain range of RCO clock periods. The calibrated RCO accuracy is proportional to the length of the clocked time. On the other hand, the size of the counter is proportional to circuit size and power consumption. A 12-bit counter is implemented as a trade-off between power, size and target accuracy.

To reduce calibration time, extensive digital and fast calibration schemes are implemented to reduce the power overhead. A total of $< 100\mu\text{s}$ calibration time is scheduled before each data packet, including e.g., DCO bank, DCO swing, PA 2nd harmonic calibration and ADPLL locking time.

4.3 Power State Machine

A power state machine, which is the main part of the always-on block, is implemented in the digital always-on block, to steer the radio into different power modes. Table 1 defines five major power states. In deep sleep mode, RCO and always-on block are switched on. In sleep mode, system clock switches from RCO to XO and MCU starts to run. In standby mode, DCO is switched on and ADPLL starts to lock. Finally, in TX mode, PA is turned on and starts to transmit, while in RX mode, the receiver chain is switched on to receive packets.

The deep sleep mode power consumption is $1.5\mu\text{W}$, including 160nW from RCO, 200nW from always on logic and $1.3\mu\text{W}$ leakage power. Leakage power is dominated by the DPLL, Power Amplifier (PA) and Digitally controlled Oscillator (DCO). Therefore, high V_t devices are used in PA and DCO to minimize leakage current. From digital part, distributed power-gating is implemented extensively, to avoid large current overshoot during power on and unknown states feeding back to DBB blocks during power off. The $1.5\mu\text{W}$ deep sleep power consumption helps to bring down the average power to μW -range, during phase II when LDO is bypassed. Moreover, the SoC can continuous work till the battery voltage drops to 0.8V , as it is directly attached to the battery. By these two factors, the battery life is extended.

Fig. 8 Receiver block diagram with NF and DC-offset sketches

Fig. 9 DC offset calibration scheme (a) block diagram; (b) timing diagram (©2016 IEEE)

4.4 Receiver Design

The receiver chain (Fig. 8) consists of a LNA with on-chip matching network, a RF mixer, a quadrature IF-mixer, a programmable gain low-pass filter (LPF), a 9-bit SAR ADC and the DBB. The corner frequency of the LPF is programmable from 500kHz to 2MHz, enabling the compliancy to multi-standards, i.e., BLE 4.0/4.2, BLE 5.0 and 802.15.4 and 4Mbps proprietary mode.

Sensitivity, the key parameter of the receiver, is dominated by the noise figure and DC-offset, while the latter of which is less obvious. The sliding IF structure relaxes the DC-offset issue, since total gain is distributed over four stages. There are two kinds of DC offset: static and dynamic. A power-on DC-offset calibration, based on SAR algorithm, is implemented to remove offset voltage caused by device mismatches and process as shown in Fig. 9(a). The RX chain is AC coupled, therefore the major static DC-offset is from the input pair of the LPF, which is then amplified by the LPF chain. Without any input signal and analog front end disabled, the DC-offset is amplified and read out at the output of the ADC by digital baseband. A current is injected into the input of the last stage in the LPF, to cancel out the DC-offset, based on the ADC output.

However, the static calibration leaves a DC-offset residue, which is 10mV determined by the I-DAC resolution in the proposed design. On the other hand, dynamic

Fig. 10 Die photo (©2016 IEEE)

DC-offset introduced by LO-coupling in the IF mixer, $1/f$ noise and other factors remain tangible and can degrade the sensitivity. A high pass filter is added in the signal chain to remove both. The corner frequency of the $1/H$ filter trades off between signal loss and group delay. The $8\mu\text{s}$ -preamble time limits the low end of the corner frequency, while the DC removal sets a frequency boundary at the high end. To resolve that, a gear-shifted $1/H$ filter is implemented as shown in Fig. 9(b). The corner frequency steps down from 1MHz to 80kHz, from preamble part to the packet data part, allowing efficient DC offset removal. Further implementation details of Fig. 9(a) can be found in [11].

4.5 Transmitter Design

The fully digital polar transmitter delivers a maximum 1dBm, 2-point modulated signal to the air. A digital ramp-up circuit is implemented to avoid PA pulling. A digital phase locked loop (DPLL) [11] with several calibration loops provide energy-efficient LO signal to TX and RX. The total calibration time, including the locking time, is $< 100\mu\text{s}$, thus meeting the BLE turn-around time $150\mu\text{s}$ for applications.

4.6 Measurement Results

The SoC is fabricated in 40nm CMOS technology and the die photo is shown in Fig. 10. Figure 11(a) shows dynamic current profile of: $1.5\mu\text{A}$ deep sleep mode (excluding MCU and RAM), $180\mu\text{A}$ sleep mode and $900\mu\text{A}$ ADPLL locking mode. Figure 11(b) shows current profile of duty cycled TX: alternating between $180\mu\text{A}$ sleep mode and 10mA transmitter mode, leading to an average power consumption of $206\mu\text{W}$ from 1V supply.

The packet error rate (PER) performance of the RX is shown in Fig. 12, with input signal level sweeping from 0dBm to -95dBm , across 40 BLE channels. The RX sensitivity reaches -93dBm for the whole BLE band, and the PER approaches to 0% for the entire RX input dynamic

1: deep sleep; 2: sleep; 3: stand-by

(a)

(b)

Fig. 11 TX measured current profile: (a) transition between different power states; (b) average current

Fig. 12 BLE 4.0 RX PER vs. input signal results (©2016 IEEE)

range. The measurement was carried out with 1V supply. The TX measurement shows in-band spur well below -30dBm with maximum 1dBm Pout. Further CBT test shows the proposed SoC is fully compliant with BLE4.0 standard, including interference test, carrier frequency drift, modulation characteristic etc.

Figure 13 shows the SoC performance with supply voltage across 0.9V to 1.2V without LDO. The RX sensitivity is -89dBm~-94dBm between 0.92V-1.2V, -75dBm when reaches minimum 0.9V; TX output power varies from -0.6dBm to 2.5dBm between 0.9V-1.2V, with FSK error

Fig. 13 TRX performance vs. VDD supply (©2016 IEEE)

Fig. 14 TX performance for BLE5.0PHY and 4Mbps proprietary mode (©2016 IEEE)

Fig. 15 Power breakdown of a heavily duty-cycled BLE wireless sensor node

< 6%. The SoC has also been tested with battery supplied, working continuously to 0.9V.

Sensitivity in other modes are also evaluated, and the results are: -94dBm in 802.15.4 mode, -92dBm in BLE5.0PHY and -85dBm in 4Mbps proprietary mode. On the transmitter side, a FSK error of 5% is measured for 802.15.4 mode, 6% for BLE5.0 PHY and an EVM of 2% for 4Mbps mode, as shown in Fig. 14.

Figure 15 shows the power breakdown of a sensor node enabled by the proposed radio, for a duty-cycled ratio of 0.34%. Even while BLE is amongst the most low power radios available, the radio power consumption is clearly dominant. For other wireless standards, like for long range outdoor sensor networks the radio peak power is only more dominant in view of battery lifetime. It can be extrapolated that with lower duty-cycle ratio than 0.34%, leakage power consumption starts to contribute to the total power consumption with heavier weight, which proves the importance of sleep mode power optimization.

Table 2 Comparison with state-of-the-art results

	This work integrated match	[5]	[6] Integrated match	[7] Differential mode	[8]	[9]	[10]
Standards	BLE 4.0/4.2 5.0PH/802.15.4, 4Mbps proprietary	BLE 4.0	BLE 4.1	BLE 4.1	BLE 4.1	BLE 4.0	BLE 4.0, 802.15.4, 802.15.6, 2Mbps proprietary
RX sensitivity	-93 dBm	-96 dBm	-93 dBm	-97 dBm	-90 dBm	-93 dBm	-93 dBm
RX ACR _{max}	25 dB	23 dB	NA	25 dB	29 dB	40 dB	24 dB
RX max input	>0 dBm	0 dBm	NA	4 dBm	1 dBm	0 dBm	>0 dBm
RX blocking	-25 dBm	NA	NA	-20 dBm	-30 dBm	-18 dBm	-30 dBm
TX P _{out}	>0 dBm	0/4 dBm	0 dBm	5 dBm	0 dBm	0.5/4 dBm	0 dBm
V _{dd}	1V–0.9V	3V	3V	3V	3V	3V	1.2V
Power diss. RX	<5.6 mW	16.5 mW	14.7 mW	18.3 mW	10.5 mW	27.75 mW	4.5 mW
TX (@0 dBm)	<8.4 mW	16.5 mW	14.7 mW	18.3 mW	12.9 mW	39.9 mW	5.7 mW
Sleep	<1.5 μ A	1.5 μ A	1.8 μ A	3.6 μ A	0.6 μ A	6 μ A	–

The proposed radio performance is summarized and compared with the state-of-the-art sensor-node candidates in Table 2. Under nominal condition, the proposed multi-standard radio offers gives highest output power, lowest active power consumption, comparable sensitivity level and optimized system architecture. Further, with the proposed two-phase power-up scheme, Fig. 4, the battery life for the proposed radio can be extended up-to 60%.

5. Conclusions

This paper explains the key specifications for IoT end nodes, power consumption and form factor. A 2.4GHz radio is introduced as a case study, showing the circuit/system design procedure and considerations to achieve low power consumption and small area. Power consumption is minimized by system planning, optimized power supply scheme and power optimization in sleep mode as well as active mode. The small form factor is made possible by highly integration of RF matching network and antenna switch. While keeping low power and small size, the proposed radio also demonstrates the state-of-the-art performance. The receiver offers -93dBm sensitivity for BLE 4.0 mode, and the transmitter delivers maximum 1dBm output. The SoC functions well with minimum 0.9V voltage supply. The compliancy to BLE4.0/4.2/5.0PH and 802.15.4 also enables short-range proximity-bases services and security.

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