SUMMARY There have recently been more and more reports on CMOS integrated circuits operating at terahertz (≥ 0.1 THz) frequencies. However, design environments and techniques are not as well established as for RF CMOS circuits. This paper reviews recent progress made by the authors in terahertz CMOS design for low-power and high-speed wireless communication, including device characterization and modeling techniques. Low-power high-speed wireless data transfer at 11 Gb/s and 19 pJ/bit and a 7-pJ/bit ultra-low-power transceiver chipset are presented.

key words: high-frequency circuit design, CMOS, millimeter wave, terahertz

1. Introduction

Millimeter wave is usually defined as the frequency range between 30 GHz and 300 GHz [1], [2]. The definition of “terahertz,” on the other hand, is more author-dependent. A definition in [3] refers to the frequency range between 0.1 THz and 10 THz. According to these definitions, the frequency range between 100 GHz and 300 GHz is both millimeter wave and terahertz. Enormous potential this frequency range offers for ultrahigh-speed communication and (sub)terahertz sensing has recently stimulated great interest. As shown in Fig. 1 [4], both wireline and wireless communication data rates are growing year by year. Notably, the rate of increase for wireless communication is much faster than wireline communication. If the rate of increase remains steady, wireless communication is expected to reach 100 Gb/s in 2020. A promising means of realizing the ultrafast wireless data rate of 100 Gb/s is to utilize this frequency range. Importantly, this target frequency range is well within reach of advanced CMOS technologies. As shown in Fig. 2 [5], the maximum operation frequency or unity-power-gain frequency $f_{\text{max}}$ of the n-type MOSFET is projected to rise steadily in the coming years according to the ITRS [7]. Also operation frequencies of millimeter-wave CMOS amplifiers are getting higher and higher, nearing 300 GHz. It should be noted that millimeter-wave designers often have to start their design from primitive device layout, device characterization and modeling as shown in Fig. 3 [4]. This is because process design kits (PDKs) available from CMOS foundries are often not validated at up-per millimeter-wave frequencies. Therefore, if one wants to design CMOS circuits for frequencies above 100 GHz, they have to study measurement and modeling, too. In this paper, we review recent achievements in our research group.

2. Device Layout and Modeling

2.1 Bond-Based Design

At millimeter wave frequencies, it is imperative that layout parasitics including resistances, capacitances and inductances (both self and mutual) be appropriately taken into consideration. However, ordinary layout parasitic extraction (LPE) tools used for chip design do not extract induc-
Electromagnetic (EM) simulation should, in principle, help here, but in practice, it is not as simple as might be expected, for interconnect structures to be simulated can be rather complicated due to modern CMOS design rules and multiple materials involved. Also only limited information about material properties required for predictive EM simulation is provided by the foundry.

A measurement-based design approach to avoiding the difficulty associated with layout parasitics is shown in Fig. 4. In this approach, every circuit component is designed to have standard transmission-line interfaces and is characterized at those interfaces. The standard transmission line has sidewalls and unwanted interference between neighboring components is minimal. Thus, all pre-characterized devices can be connected with each other at the interfaces by just bonding as shown in Fig. 4. No post-layout parasitic extraction is necessary. We called this type of design “bond-based design” [8], [9].

2.2 Power-Line Decoupling

Power-supply line decoupling for wideband millimeter-wave circuits is a major challenge since commonly-used decoupling capacitors exhibit self-resonance. Decoupling capacitors become inductive above the self-resonant frequency, and power-supply rail shunting (Fig. 5) does not work reliably at millimeter-wave frequencies. To solve this problem, transmission line with very low characteristic impedance can be utilized [10], [11], as shown in Fig. 6. It serves as a wideband decoupling device as well as power line. Why can a transmission line with low characteristic impedance be a decoupling device? Generally, the input impedance of a terminated lossy transmission line on a Smith chart spirals into its characteristic impedance $Z_0$, regardless of the far-end termination when its length or the frequency is swept [12], as shown in Fig. 7. The lossier (larger attenuation constant), the faster the input impedance falls onto the characteristic impedance. Obviously, if $Z_0 \approx 0 \Omega$, the input impedance also approaches $0 \Omega$, which is the desired behavior. We call this type of transmission line de-
Fig. 7  Input impedance $Z_{in}$ of a lossy transmission line converges at its characteristic impedance $Z_0$ as its length $l$ or the frequency $f$ is swept, regardless of how the far end of the line is terminated. In this example, $Z_0 \approx 10 \Omega$, $5 \mu m \leq l \leq 5 \text{mm}$, and $f = 60 \text{GHz}$.

signed to have as low a characteristic impedance as possible as “the zero-Ohm transmission line (0-$\Omega$ TL)” [13]. The characteristic impedance should be less than 1 $\Omega$ for best decoupling performance [10]. How can we achieve low characteristic impedance? Characteristic impedance $Z_0$ at an angular frequency $\omega$ is given by

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}},$$  \hspace{1cm} (1)$$

where $R$, $L$, $G$ and $C$ are the per-unit-length RLGC parameters [12] (Fig. 8). Here, the propagation constant $\gamma$ is given by

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)},$$  \hspace{1cm} (2)$$

and $\alpha = \Re(\gamma)$ and $\beta = \Im(\gamma)$ are the attenuation and phase constants, respectively. Since the combination of low dc resistance (for low-loss dc power supply) and high RF attenuation (large $\alpha$) makes a good decoupling device [14], [15], the per-unit-length resistance $R$ should be as small as possible for low dc loss and capacitance $C$ should be as large as possible for small $|Z_0|$ and large $\alpha$. In CMOS process, 0-$\Omega$ TL is typically built as shown in Fig. 9. Here, thick metal layers are used for the main dc path for small $R$. Three types of capacitors are used to give a large $C$: MIM (metal-insulator-metal) parallel-plate capacitors, MOM (metal-oxide-metal) interdigital capacitors and MOS (metal-oxide-semiconductor) capacitors. Since the 0-$\Omega$ TL is difficult to characterize due to its low $Z_0$, we characterized it by measuring its input impedance $Z_{in}$ using specially designed test structures [14]. Measured input impedances of open and shorted stubs of various lengths are shown in Fig. 10. $Z_{in}$ stays below 2 $\Omega$, which is nearly short, up to 325 GHz. The longer the stub, the faster $Z_{in}$ falls onto $Z_0$.

Since $Z_0$ of power distribution transmission line can be used as a performance figure-of-merit [10], Table 1 shows comparison of $|Z_0|$ of CMOS decoupling power lines.

|          | $|Z_0|$ @60 GHz | $|Z_0|$ @300 GHz |
|----------|----------------|-----------------|
| [11]     | 2.2 $\Omega$   | -               |
| [13]     | 1.5 $\Omega$   | -               |
| [16]     | 1.6 $\Omega$   | -               |
| [17]     | “around 1 $\Omega$” | -            |
| Our work | 0.7 $\Omega$   | 1.6 $\Omega$   |

2.3 De-Embedding

At above 100 GHz, TRL (through-reflect-line) de-embedding is commonly used [18]. In particular, multiline TRL [19] gives reasonable de-embedding results since weighted averaging over multiple lines is performed.

The $Z_0$-referenced $S$ matrix of a length, $\Delta L$, of transmission line is given by

![Fig. 8](image-url)  RLGC model of a unit-length transmission line section.

![Fig. 9](image-url)  Structure of the 0-$\Omega$ TL.
Fig. 10  Input impedance $Z_{in}$ of open (red) and shorted (blue) stubs (Fig. 7) of lengths 33 μm, 66 μm, 99 μm, 132 μm, 198 μm, 297 μm, and 396 μm at 1–170 GHz and 220–325 GHz.

Fig. 11  Frequency-dependence of $S_{21}$ of moderately lossy transmission line of lengths $\Delta L_1$ and $\Delta L_2$. $\alpha \Delta L = -\ln |S_{21}|$ and $\beta \Delta L = -\arg S_{21}$.

$$S_{(Z_0)} = \begin{bmatrix} 0 & e^{-\gamma \Delta L} \\ e^{\gamma \Delta L} & 0 \end{bmatrix}$$  \hspace{1cm} (3)

$$= \begin{bmatrix} e^{-\alpha \Delta L}e^{-\beta \Delta L} & 0 \\ 0 & e^{-\alpha \Delta L}e^{\beta \Delta L} \end{bmatrix}.$$  \hspace{1cm} (4)

The loci of transmission characteristics $S_{21}$ of moderately lossy lines will look as shown in Fig. 11 on a polar chart. The attenuation constant $\alpha$ can be extracted from the magnitude $|S_{21}|$ and the phase constant $\beta$ from the argument $\arg S_{21}$. In the context of applying TRL, $\Delta L$ corresponds to the line-length difference between a pair of lines.

Actual transmission lines (except those for decoupling) are designed to be as low-loss as possible. As a result, $|S_{21}| = e^{-\alpha \Delta L}$ [see Eq. (4)] stays close to unity for typical values of $\Delta L \leq 1$ mm. In such a case, precise estimation of $\alpha$ is difficult especially at high frequencies where all sorts of “noise” present in measured $S$ parameters can be large and nearly comparable to $1 - |S_{21}|$. Figure 12 shows measured $\alpha$’s extracted by multiline TRL from different line sets. Not only are the resultant $\alpha$’s highly dispersed especially at frequencies above 140 GHz, also the frequency dependence is very erratic. In fact, similar erratic behavior of $\alpha$ at millimeter-wave frequencies can often be found in published papers [20]–[22]. Such erratic behavior cannot easily be reproduced by EM simulation. Aside from measurement equipment noise, spurious modes [23] and crosstalk [24] might be contributing to the “noise” in measured $S$ parameters. To suppress the noise and extract the attenuation constant associated with the lowest-order propagation mode, the longest line should be very long, leading to a much larger $\Delta L$ value than a typical value of about 1 mm. We tried multiline TRL with the line sets shown in Table 2, the longest line being 8 mm. The chip micrograph is shown in Fig. 13. Estimated $\alpha$ and $\beta$ are shown in Fig. 14 [25]. The larger the $\Delta L_{\text{max}}$, the more well-behaved $\alpha$ is. When $\Delta L_{\text{max}} = 8$ mm, the $\alpha$ is very well-behaved. This result suggests that precise de-embedding and reference-plane shifting are possible only if very long lines are used in multiline TRL.

2.4 Parameter Extraction for EM Field Simulation

To perform accurate electromagnetic (EM) field analysis at millimeter wave and terahertz frequencies, precise material parameters are required. Although the nominal values of metal conductivities and the real parts of dielectric per-
mittivities are provided by foundries, other parameters that critically affect the performance, including complex dielectric permittivities and effective thicknesses of interconnect layers are generally not provided. Thus, we developed a systematic method of calibrating process parameters, applicable up to terahertz frequencies [26], [27]. Since propagation constants of transmission lines extracted by multiline TRL using long lines are fairly reliable [25], propagation constants are utilized for extracting process parameters together with the estimates of characteristic impedance [28], [29]. A cross-sectional structure of a standard CMOS interconnect layers is shown in Fig. 15. After applying TRL, process parameters are extracted following the flow chart shown in Fig. 16. The propagation constants in the entire measurement frequency range and the RLGC parameters (Fig. 8) at low frequencies are used to determine process parameters.
By using four types of microstrip lines shown in Fig. 17, we determined process parameters. Attenuation constants and phase velocities obtained from measurement and EM simulation are compared in Fig. 18 [27]. Measured capacitance of an on-chip interdigital MOM capacitor is compared with that obtained from EM simulation in Fig. 19. The characteristics calculated with the calibrated process parameters show better agreement with those obtained from the measurement.

2.5 MOSFET Parasitic Resistances at Millimeter Wave

Predictive circuit simulation is possible only if device models that accurately reproduce measurement results are available. To build a reliable MOSFET model, parasitic resistances in device layout, shown in Fig. 20, have to be estimated in terahertz region. The parasitic resistances at terahertz frequencies are generally different from dc values due to non-quasi static effects. To extract the parasitic resistances, “cold-bias de-embedding” or the “cold-FET method” [30] is applied.

Theoretically, since the channel resistance is proportional to the reciprocal of the overdrive voltage (gate voltage minus threshold voltage), parasitic resistances can be extracted by mathematically zeroing the channel channel resistance by extrapolating the overdrive voltage to infinity. This is the essence of cold-bias de-embedding. In RF cold-bias de-embedding, real parts of the impedance matrix of a MOSFET at a low frequency is used. However, since real

measurement data show dispersion, we proposed a new extraction method [31]. In this method, measured data up to 110 GHz were first smoothed out as shown in Fig. 21 before further processing. Figure 22 shows comparison of extracted resistances with and without smoothing as a function of the gate voltage. Clearly, smoothing in the previous step has given more well-behaved result. Now the extracted re-
Parasitic resistances

Fig. 20  Schematic layout of a MOSFET and its equivalent circuit highlighting parasitic resistances.

Fig. 21  Measured $S_{22}$ at 0.5–110 GHz under different bias conditions. Immittances that are located near the center of the reflection-coefficient plane (Smith chart) are more reliable and less susceptible to measurement uncertainties than those located far from the center because of the mathematical form of the linear fractional transformation that relates reflection coefficients to immittances. $S_{22}$ at 500 MHz are in the unreliable region.

Fig. 22  Channel resistance ($R_{ch}$) plus parasitic resistances ($R_D + R_S$) extracted from raw and smoothed data at 500 MHz versus the gate voltage $V_{GS}$.

Fig. 23  Extraction of parasitic resistance $R_D + R_S$ by linear extrapolation ($V_{GS} - V_{th})^{-1} \rightarrow 0$ works only if the value of $V_{th}$ is the millimeter-wave value of 0.5 V. The dc threshold voltage is 0.4 V.

Fig. 24  $S$ parameters of a 65-nm NMOSFET at 0.5–330 GHz (not including 170–220 GHz).

Resistance ($R_D + R_{ch} + R_S$) is expected to be a linear function of the reciprocal overdrive voltage $(V_{GS} - V_{th})^{-1}$. But in practice, that turned out not to be the case, if the value of $V_{th}$ was equal to the dc value of 0.4 V, as shown in Fig. 23. We, therefore, introduced the millimeter-wave threshold voltage (mmw $V_{th}$), equal to 0.5 V, which makes $R_D + R_{ch} + R_S$ a linear function of $(V_{GS} - V_{th})^{-1}$. The parasitic resistance $R_D + R_S$ can then be extracted reliably by linear extrapolation $(V_{GS} - V_{th})^{-1} \rightarrow 0$, as shown in Fig. 23, which amounts to bringing $R_{ch}$ to zero. After reliably extracting the parasitic resistances, we successfully developed a MOSFET model applicable to 300-GHz nonlinear simulation. Comparison of $S$ parameters obtained from simulation with the new model and measurement is shown in Fig. 24. The agreement is reasonable throughout the drain and gate voltage ranges of 0 V to 1.2 V.
3. Gain and Noise Optimization of Small-Signal Amplifier

At terahertz frequencies, many (≥ 5) gain stages are required to build amplifiers due to the limited MOSFET gain (≤ 5 dB). However, in general, optimization of many-stage amplifiers is difficult because the design of each matching network cannot be done independently of others due to non-negligible reverse isolation (S_{12}) of MOSFETs. Accordingly, computational optimization is necessary.

In our approach, small-signal transfer functions of all constituent devices with geometrical parameters are first modeled. Then, the overall transfer function of the amplifier is calculated. After giving initial parameter values (for example, by [32]) to the constituent devices, a conjugate-gradient engine maximizes an objective function as shown in Fig. 25 [33]. For ultrahigh-speed communication at 10 Gb/s or faster, amplifiers with flat gain and flat group delay over a very wide frequency range are required. In our optimization procedure, inter-stage matching networks are optimized first, and then the input and output matching networks are optimized, as shown in Fig. 26.

Note that the objective function can be defined to search for lower noise figure (NF) or for higher gain. The optimization procedure can also be tuned depending on the objective. The gain can be maximized by realizing simultaneous conjugate matching at the input and the output if the amplifier is unconditionally stable. On the other hand, noise figure (or equivalently, noise factor) is minimized when the source impedance has a certain optimal value. Generally, conditions of conjugate power matching and minimum noise figure are not the same. Therefore, noise figure of the first gain stage is usually minimized in microwave low-noise amplifiers (LNAs) since noise figures of the succeeding stages do not affect the overall noise performance very much. However, the situation is somewhat different in terahertz amplifiers. The typical gain per stage at terahertz frequencies is so low that the noise figure of the second and even the third stage may affect the overall noise performance of a multistage amplifier. Generally, the higher the gain of the first gain stage, the less the impact of the noise figures of the later stages on the overall noise figure [34]. Therefore, conjugate power matching at the input port of the first stage might give a smaller noise figure than does the ordinary “noise matching” strategy.

We used the four-stage common-source amplifier, shown in Fig. 27, as a test vehicle and tested two design strategies in computational optimization. The design targets were a center frequency of 135 GHz and a fractional bandwidth of over 20%. The results of applying conjugate matching and noise matching are shown in Fig. 28. The gain (S_{21}) of the noise-matched case is lower than the conjugate-matched case as expected. But the NF of the noise-matched case is not significantly better than the conjugate-matched case. This is in stark contrast with ordinary low-GHz amplifiers. As illustrated in this example, the conventional low-noise design might not be optimal for terahertz design.
Fig. 29  Concept of the area-saving "fishbone layout."

Fig. 30  Chip micrographs of an eight-stage 160-GHz amplifier. Shunt stubs are made of narrow 71-Ω transmission lines. Wider 50-Ω transmission lines are used for signal I/O.

Fig. 31  Measured S parameters of the amplifier in Fig. 30.

Table 3  Comparison of CMOS G-band amplifiers.

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<td>40 nm CMOS</td>
<td>9/Single-Ended</td>
<td>210</td>
<td>13</td>
<td>130 x 103</td>
<td>10.5</td>
<td>43.5</td>
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<tr>
<td>IEEE MWCL [2]</td>
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<td>3/Differential</td>
<td>144</td>
<td>3°</td>
<td>480 x 100</td>
<td>20.6</td>
<td>40.7</td>
</tr>
<tr>
<td>APMC '13 [5]</td>
<td>65 nm CMOS</td>
<td>4/Differential</td>
<td>147</td>
<td>13°</td>
<td>580 x 200</td>
<td>7.1</td>
<td>29.4</td>
</tr>
<tr>
<td>This work</td>
<td>40 nm CMOS</td>
<td>8/Single-Ended</td>
<td>160</td>
<td>41</td>
<td>190 x 123</td>
<td>14.9</td>
<td>241.8</td>
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*Estimated from chip micrograph

4. Compact Layout Technique

Many-stage amplifiers for terahertz frequencies tend to occupy a large area since inter-stage matching networks consist typically of several passive devices that are much larger than MOSFETs. To realize cost-effective chips, area reduction is important. In order to reduce the area of amplifiers, we proposed the “fishbone layout” [35], shown in Fig. 29. In this technique, transmission line stubs used in matching networks are arranged regularly at narrow spacings, and the transmission lines themselves are designed to be narrow, thereby reducing the footprint. A chip micrograph of an eight-stage 160-GHz amplifier with fishbone layout is shown in Fig. 30. The core size is as small as 190 x 123 μm². Measured small-signal characteristics of the 160-GHz amplifier are shown in Fig. 31. The peak gain is 14.9 dB at 160 GHz with the power consumption of 117 mW at the supply voltage of 0.9 V. Performance of CMOS G-band (140–220 GHz) amplifiers is compared in Table 3.

5. 130-GHz CMOS Transceiver Chipset

Terahertz frequencies are most suitable for realizing ultrafast communication taking advantage of the abundant available bandwidth. Figure 32 shows a block diagram of a 130-GHz-band ASK (amplitude shift keying) transceiver [36]. While ASK has a low spectral efficiency (data rate per unit bandwidth), since it does not make use of phase for modulation, circuits can be implemented fairly easily, even without PLL and baseband circuitry including ADC/DAC. ASK, therefore, is ideally suited for low-power transceivers. Figure 33 shows a schematic diagram of the ASK transmitter. It consists of a 130-GHz push-push oscillator, an ASK modulator and a power amplifier (PA). The ASK modulator adopts parallel switches with a section of transmission line. It has the advantages of consuming no dc power and yet giving a sufficiently high on/off ratio with low insertion loss.

To realize a date rate of 10 Gb/s or faster with ASK, approximately 20-GHz bandwidth with small group delay variations is required not only of the PA but also of other circuit blocks from the baseband input through to the antenna,
Fig. 32 Block diagram of the 130-GHz ASK transceiver chipset.

130GHz push-push oscillator

Fig. 33 Schematic diagram of the 130-GHz ASK transmitter.

Fig. 34 Modulator’s gain $S_{21,\text{MOD}}$ becomes lower at higher frequencies due to the modulator. To compensate for that and make the overall transmitter (Tx) gain $S_{21,\text{TX}}$ flat, the input matching network of the PA is tuned.

including the modulator. Figure 34 shows a schematic that includes the modulator and the PA. In the modulator, the transmission line is lossier at higher frequencies. If the gain of the PA is flat, the overall gain becomes lower at higher frequencies due to the modulator. The input matching network of the PA is tuned to compensate for the high-frequency loss. Figure 35 shows the simulated small-signal gain of the PA before tuning and the transmitter (Tx) after tuning. 3-dB bandwidth of 18 GHz was achieved. Figure 35 also shows measured characteristics of the PA without the tuning. The saturated output power was 8.6 dBm and the power-added efficiency (PAE) was 7.4%.

The power consumption of the receiver (Rx) shown in Fig. 32 was larger than that of the transmitter. This was because the per-stage gain of the amplifier was so low at terahertz frequencies that many stages were required to achieve sufficient gain. The PA in Fig. 32 has six gain stages and the LNA has ten gain stages. Low-power design of wideband LNA, therefore, is important.

Here we consider the strategy for low-power design at the device level. Figure 36 shows constant-$f_{\text{max}}$ and constant-power contours on the $V_{GS}$-$V_{DS}$ plane. Both $f_{\text{max}}$ and the power dissipation become higher with $V_{DS}$ and $V_{GS}$, but somewhat differently. For example, Fig. 37 shows the $f_{\text{max}} = 150$ GHz contour with the vertical axis being the power. Clearly, an optimal bias condition exists that minimizes the power for a given value of $f_{\text{max}}$. We refer to this bias condition as “the power-efficient bias” [5]. Figure 38 shows the power-efficient bias on the $V_{GS}$-$V_{DS}$ plane. By choosing such a bias condition, a desired performance (designated by $f_{\text{max}}$) is obtained with the lowest possible power.
Fig. 37  Power consumption of a 40-nm NMOSFET (per gate width) on the $f_{\text{max}} = 150$ GHz contour.

Fig. 38  Power-efficient bias (red curve) gives the lowest possible power for a given transistor performance, designated by $f_{\text{max}}$.

Shown in Fig. 39 is the ten-stage LNA in the block diagram in Fig. 32. The gain of this LNA can be controlled through changing the bias voltages. Figure 39 also shows the measured small-signal gain under different bias conditions. Figure 40 shows the power consumption as a function of the gain-bandwidth product (GBW) [37]. Here the GBW changes due mainly to the change in gain. Thus, the power-efficient bias helps in finding an optimal bias condition for power reduction.

The 130-GHz transceiver chipset was fabricated using a 40-nm CMOS process. Figure 41 shows the micrographs of the transmitter and the receiver. Wireless communication test was performed with two sets of probe stations, waveguide probes, and horn antennas. An eye diagram at 11 Gb/s and the bit error rate are shown in Fig. 42. The bit error rate was $10^{-9}$ at 11 Gb/s. The antennas were 3 m apart as shown in Fig. 43. The power consumption of the Tx and the Rx were 77 mW and 132 mW, respectively. The power consumption per bit rate of CMOS transceivers is plotted as a function of communication distance in Fig. 43 [36]. Our transceiver chipset consumed 19 pJ/bit and is most energy-efficient for the communication distance of 1 m and longer. While ASK is not very suitable for environments where multipath propagation occurs, it can realize very low-power communication under controlled circumstances.
6. ASK Communication without PA

For extremely short-range communication (≤ 10 cm), the transmitter can be built only from an oscillator and a modulator, without a PA. Micrographs of PA-less 80-GHz and 100-GHz transmitters are shown in Fig. 44 [38]. Because of the PA-less architecture, the transmitters are very small and low-power. Figure 45 shows the data rate versus communication distance, together with performance summary. The 80-GHz chip achieved the data rate of 15.4 Gb/s at a 2-cm distance. The power consumption was 107.6 mW and the energy per bit was as low as 7 pJ/bit.

7. Conclusions

Since the first microwave link installed by Marconi in 1932, the carrier frequency used for wireless communication has risen roughly exponentially with time [39]. If this trend is to continue, the frequency range of 300 GHz to 3 THz will be used for wireless communication by the end of 2010s. As a matter of fact, an experimental demonstration of wireless link at 300 GHz have already been reported [40]. The circuit was fabricated with InP HEMT technologies [40].

While CMOS technology is making steady progress, the state of the art does not seem to be good enough for realizing amplifiers at 300 GHz and above. According to Fig. 1, a wireless data rate of 100 Gb/s is expected around 2020. Given the fact that the pace of CMOS technology advancement is slowing down, the role of design in improving circuit performance is expected to become more and more important [41].

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