A Novel Hardware Architecture of Intra-Predictor Generator for H.264/AVC Codec

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SUMMARY The intra-prediction unit is an essential part of H.264 codec, since it reduces the amount of data to be encoded by predicting pixel values (luminance and chrominance) from their neighboring blocks. A dedicated hardware implementation for the intra-prediction unit is required for real-time encoding and decoding of high resolution video data. To develop a cost-effective intra-prediction unit this paper proposes a novel architecture of intra-predictor generator, the core part of intra-prediction unit. The proposed intra-predictor generator enables the intra-prediction unit to achieve significant clock cycle reduction with approximately the same gate count, as compared to Huang's work [3].

key words: H.264/AVC, intra predictor, hardware implementation, architecture level optimization

1. Introduction

Intra-prediction is one of the two prediction parts in H.264/AVC standard. To reduce the amount of transmitted data, pixel values are predicted based on previously encoded and reconstructed samples in the same frame [1]. The intra-prediction unit calculates predicted pixel values for all the intra-modes and then selects the best mode that produces minimum SAD (Sum of Absolute Differences). For vertical and horizontal modes of intra-prediction, there is no arithmetic operation because predicted pixel values are simply propagated values of neighbor pixels [2]. For other directional modes, however, predicted pixel values are determined by calculating average of the two neighboring pixel values or weighted average of the three neighboring pixel values. For design of an efficient intra-prediction unit, reduction of the generation time of predicted pixel values for these directional modes is critical. In the literature, several works [3]–[5] have dealt with intra-prediction. In this paper, a reconfigurable architecture of the intra-predictor generator for the intra-prediction unit is proposed. The performance of the intra-prediction unit is compared with Huang’s work [3] to show the superiority in terms of processing rate and gate count.

The rest of this paper is organized as follows. The various modes of intra-prediction are introduced in Sect. 2. Section 3 describes the proposed architecture of the intra-predictor generator with reference to Huang’s architecture [3]. In Sect. 4, the results of the hardware implementation are presented followed by the conclusions in Sect. 5.

2. Intra-Prediction

For the intra-prediction with a 16 × 16 macroblock in 4:2:0 data format, sixteen 4 × 4 blocks or a single 16 × 16 macroblock is formed with the luminance component, and two 8 × 8 blocks are formed for the chrominance component. The two types of modes in intra-prediction for the luminance component are Intra4 × 4PredMode which consists of nine prediction modes for every 4×4 block, and Intra16 × 16PredMode including four prediction modes for every 16 × 16 macroblock. Four prediction modes for the chrominance component are identical with the four modes of Intra16 × 16PredMode, i.e., vertical mode, horizontal mode, DC mode, and plane mode.

Huang’s work presents a complete hardware implementation of intra-prediction unit, as opposed to other published works involving only part of it. Thus, Huang’s work is our main concern for comparison with our work. Also, comparison of the proposed intra-predictor generator with Huang’s one is mainly for Intra4×4PredMode of the luminance component, because it involves more than half of all the intra-modes and takes most of processing time for the intra-prediction. Figure 1 shows the nine modes in Intra4×4PredMode. For vertical and horizontal modes, intra-predictor generator predicts current 4 × 4 block as a propagation of neighbor pixels in each direction.

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Fig. 1 Nine intra-prediction modes of Intra4 × 4PredMode for 4 × 4 luminance component.
For the other six directional modes, average value of the two neighbor pixels or weighted average value of the three neighbor pixels is computed along different directions. For DC mode, average value of neighbor pixels is used for prediction.

3. Architecture of Intra-Predictor Generator

The intra-prediction unit mainly consists of three functional blocks for 'Intra-Predictor Generator’, 'Buffers’, and 'Mode Decision’, as shown in Fig. 2.

The 'Intra-Predictor Generator' block calculates the predicted pixel values for all the intra-modes. The 'Buffers' block is required for pipelining of 'Intra-Predictor Generator' and the 'Mode Decision' block determines the best intra-mode.

3.1 Intra-Prediction by Intra-Predictor Generator

To explain the proposed architecture of the 'Intra-Predictor Generator' for the intra-prediction unit, an exemplar mode 3 operations of Intra4 × 4PredMode is explained as follows.

For mode 3, the weighted average of the three neighbor pixels from diagonal down-left direction is used for each pixel value $P_{MN}$ corresponding to the position of $M$-th row and $N$-th column in a $4 \times 4$ block. For example the predicted pixel values corresponding to $P_{11}$, $P_{12}$, $P_{13}$, and $P_{14}$ can be obtained as

\[
\begin{align*}
P_{11} &= (A + 2B + C + 2) \gg 2 \\
P_{12} &= (B + 2C + D + 2) \gg 2 \\
P_{13} &= (C + 2D + E + 2) \gg 2 \\
P_{14} &= (D + 2E + F + 2) \gg 2
\end{align*}
\]

The upper right neighbor pixel of $P_{11}$ in Fig. 3 taking the value ‘B’ is multiplied by ‘2’ and added with ‘A’, ‘C’, and the alphanumeric number ‘2’. Since the result of the summation is about four times the neighbor pixel value, the shift-right by ‘2’ operation is taken to divide it by four. The
addition of ‘+2’ before the shift operation is for round-off operation.

3.2 Huang’s Intra-Predictor Generator

Figure 4 shows the configuration of Huang’s four-parallel units in the intra-predictor generator [3]. The reconfigurable architecture can support all kinds of intra-mode predictions in H.264/AVC standard. Each unit consists of three adders and a unit for round-off and shift. The four parallel units in this architecture can generate four predicted pixel values in a clock cycle.

3.3 Proposed Architecture of Intra-Predictor Generator

Figure 5 shows the proposed architecture of intra-predictor generator. It includes fifteen adders and facilitates all kinds of intra-mode prediction with different configurations. I1, I2, ..., I16 denote the input values of the adders in the first stage, and O1, O2, ..., O16 indicate the final output values. Table 1 shows the input values Ij (1 ≤ j ≤ 16) for each directional mode of Intra4×4PredMode. The input pixel values A, B, ..., M represent the neighbor pixel values in Fig. 3. Table 2 lists the output values Oj (1 ≤ j ≤ 16) as the predicted pixel values for each pixel position. For example, only O9 to O15 are used for mode 3. In case of the output O12, it is repeatedly used for mode 3 as the predicted pixel values corresponding to the pixel positions P14, P23, P32, and P41.

![Table 1](https://example.com/table1.png)

As shown in Table 2, the proposed intra-predictor generator can compute all the predicted pixel values in a 4 × 4 block for six directional modes in a single clock cycle by repeated use of pixel values. On the other hand, Huang’s architecture is fixed to compute four pixel values in a clock cycle by row-by-row fashion, requiring four clock cycles for a 4 × 4 block.

In the proposed architecture, ‘carry-in’ is set to 1 for the first stage adders to avoid the use of round-off operators. Since each adder in the second stage takes two ‘carry-in’s from two adders in the first stage, the addition of the number ‘2’ is performed as a result. Figure 6 illustrates the configuration of intra-predictor generator for mode 3 of Intra4×4PredMode with the outputs as the predicted pixel values. With the final shift-right by ‘2’ operations the intra-predictor generator produces predicted pixel values in a 4 × 4 block.

![Table 2](https://example.com/table2.png)

![Fig. 6](https://example.com/fig6.png)
4. Implementation Results

In order to evaluate the performance of the intra-prediction unit including the proposed intra-predictor generator, required prediction clock cycles for one 16 × 16 macroblock and the gate count of intra-prediction unit are calculated. The intra-prediction unit was synthesized with ANAM 0.18 μm CMOS technology. For intra-prediction, the proposed intra-predictor generator can reduce the number of clock cycles necessary for Intra4×4PredMode with the luminance component up to a quarter compared with Huang’s architecture.

The number of clock cycles necessary for a 16 × 16 macroblock intra-prediction by the proposed intra-prediction unit including intra-predictor generator is listed in Table 3. In spite of three more adders used for the proposed intra-predictor generator in comparison with Huang’s one, the gate count is almost the same. It is because the gate count of each adder is lower than 1% of the total gate count of intra-predictor generator, so its contribution to the overall gate count is not significant. As a whole, the gate count of the proposed intra-predictor generator is about 13% (14695/12945) larger than that of Huang’s one. Considering 25% reduction [(960 − 720)/960] of prediction clock cycles, proposed intra-predictor generator is quite competitive.

The intra-prediction unit proposed by Suh et al. [4] requires only 544 cycles for a 16 × 16 macroblock, at the expense of large gate count mainly due to two parallel intra-predictor generators, one for Intra4×4PredMode and the other for Intra16×16PredMode and the chrominance component. Jin and Lee’s intra-prediction unit [5] requires 475 cycles only, but it does not support plane mode which requires most complicated calculation. Also they did not show the gate count of parallel intra-predictor generators and associated pipelined architecture, which is typically associated with large gate count increase. All the prediction cycles of the previous works [3]–[5] in Table 3 are only for intra-prediction unit.

Required clock frequency for intra-prediction unit including the proposed intra-predictor generator for 720 × 480 (30 fps) format video can be calculated as follows

\[
\text{Required clock frequency (cycles/sec)} = \frac{(45 \times 30) \text{ macroblocks/frame} \times 30 \text{ frames/sec}}{720 \text{ cycles/macroblock}} = 29.16 \text{ MHz}
\]

Similarly, the required clock frequency for other type of video can be calculated.

5. Conclusions

This paper proposed an efficient hardware architecture of the intra-predictor generator for intra-prediction unit in H.264/AVC video codec. Hardware implementation of the proposed intra-predictor generator demonstrated quite competitive performance in terms of required clock cycles and gate count, as compared to those of previously published works [3]–[5].

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References