PAPER

Parallel Parity Checksum and Syndrome Generation for Digital Video and Audio Transmission over Cable Channel*

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SUMMARY The ITU-T J.83 Annex B is a widely adopted standard in North America for digital video and audio transmission over coaxial cable. This paper proposes a new parallel processing architecture of the parity checksum generator and syndrome generator specified in the standard for packet synchronization and error detection. The proposed parallel processing architecture removes the performance bottleneck occurring in the conventional serial processing architecture, leading to significant decrease in processing time for generating a parity checksum in transmitter and a syndrome in receiver. Implementation results show that the proposed parallel processing architecture reduces the processing time by 92% for parity checksum generation and by 81% for syndrome generation over the conventional serial processing architecture.

key words: ITU-T J.83 annex B, parallel parity checksum, parallel syndrome

1. Introduction

The ITU-T J.83 Annex B standard provides a specification for the transmission of digital video and audio signals over coaxial cables [1]. This specification, named digital multi-programme systems for television, sound, and data services for cable distribution, is being widely used in North America [2], [3].

Figure 1 shows the basic block diagram of the transmission system specified in the standard [1]. The input data of the transmission system is an MPEG-2 Transport Stream (TS) consisting of a continuous flow of 188 byte lengthy packets; one byte packet header for packet synchronization and the 187 bytes of MPEG-2 video and auxiliary data [4]. The transmission system consists of three main parts. The MPEG framer is for packet error detection as well as synchronization. The FEC encoder and decoder are for providing acceptable data quality. Lastly, the QAM modulator and demodulator are for robust transmission over cable channels.

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Fig. 1 Basic block diagram of MPEG-2 TS transmission systems.

The MPEG framer is comprised of a parity checksum generator in the transmitter and a syndrome generator in the receiver. In the conventional systems, the generators are usually implemented by simple shift registers at the cost of low processing rate [1], [5]. In order to keep up the pace with the FEC encoder and decoder and the QAM modulator and demodulator, the generators should operate eight times as fast as the clock speed [5]. However, the increased clock speed leads to higher power consumption. Moreover, it causes a serious implementation problem with the devices in a limited clock speed, such as Field-Programmable Gate Arrays (FPGAs).

Other feasible approach is to increase the processing speed by replacing the conventional serial processing architecture with its parallel counterpart. The example of this approach is the use of the Cyclic Redundancy Check (CRC) circuits that are frequently found in the literatures [6]–[8], but few studies on the parallel processing architecture complying with the ITU-T J.83 Annex B standard have appeared in the literature. This paper proposes a new parallel processing architecture of the parity checksum generator and syndrome generator complying with ITU-T J.83 Annex B. The architectures are derived by obtaining matrix forms of the polynomial expressions specified in the standard and performing matrix computations.

This paper is organized as follows. Section 2 introduces the serial processing architecture of the parity checksum and syndrome generator specified in the standard. In Sects. 3 and 4, the parallel parity checksum generator and the parallel syndrome generator are explained. Section 5 discusses comparisons of implementation results. Finally, Sect. 6 concludes this paper.

2. Parity Checksum/Syndrome Generator for ITU-T J.83 Annex B Standard

The parity checksum generator and the syndrome generator specified ITU-T J.83 Annex B standard have a processing rate of 1-bit datum per clock cycle. The serial processing architecture in Fig. 2 for parity checksum generation in transmitter consists of four blocks Linear Feedback Shift Register (LFSR) block, syndrome generation block, FIR filtering block, and offset addition block.

For an encoding operation, the LFSR block is first initialized, so that all the memory elements represented as Z^{-1}

contain zero values. The 187 bytes (1496 bits) data of the MPEG-2 TS Packet (TSP) payload are then shifted into the LFSR block. By the switch 1 a byte consisting of eight zeros is appended after the 1496 bits of payload message sequence is received. The syndrome generation block computes 8-bit syndrome by seven additional shifts. The 8-bit syndrome passes through the FIR filtering block, which is initialized to an all-zero state prior to the introduction of the 8-bit syndrome over the last 8-bit time period. Finally, an offset of 67_{HEX} is added to this syndrome results to obtain encoder parity checksum output.

The serial processing architecture for syndrome generation in receiver consists of LFSR block and syndrome

Fig. 2 Serial processing architecture for parity checksum generation in transmitter.

Fig. 3 Serial processing architecture for syndrome generation in receiver.

generation block as shown in Fig. 3. The two blocks are the same as those of the parity checksum generator except the absence of the switch 1 in the LFSR block, which is indicated by the dotted box. For decoding operation, TS comes into the LFSR block. When the preceded 1496-bit data and 8-bit parity checksum are valid, the syndrome generation block produces the sync byte 47_{HEX}. The receiver synchronizes a packet and detects packet error by identifying the value of the sync byte.

3. Parallel Processing Architecture for Parity Checksum Generation

The processing rate of parity checksum generator can be increased by replacing the serial processing architecture with a parallel processing architecture. In this section, a parallel processing architecture for parity checksum generation, complying with ITU-T J.83 Annex B standard, is designed.

3.1 Polynomial Representation of the Serial Parity Checksum Generator

The serial parity checksum generator can be described by the polynomial representation. It is a well known method to represent binary sequences [9]. Let 1504-bit data of the MPEG-2 TSP message sequence, including the last byte consisting of eight zeros, be $M = (m_{1503}, m_{1502}, \dots, m_0)$, where $m_i \in GF(2)$, $i = 0, \dots, 1503$ and $m_j = 0$, $j = 0, \dots, 7$. Also let the 8-bit parity checksum sequence be $P = (p_7, p_6, \dots, p_0)$, where $p_i \in GF(2)$, $i = 0, \dots, 7$. Then the message and parity checksum sequences are expressed as coefficients of message polynomial $m(X) = m_{1503}X^{1503} + m_{1502}X^{1502} + \dots + m_8X^8$ and parity polynomial $p(X) = p_7X^7 + p_6X^6 + \dots + p_0$, respectively. Likewise, the polynomial $l(X)$ representing the output sequence of LFSR block of the transmitter in Fig. 2 is expressed as

$$l(X) = \sum_{k=0}^{1503} l_k X^k = Q\left(\frac{X^8 m(X)}{g(X)}\right) \quad (1)$$

where the generator polynomial $g(X)$ is specified as $g(X) = X^8 + X^6 + X^5 + X + 1$ and the operator $Q(\cdot)$ gives the quotient obtained by polynomial division [1]. The output polynomial $s(X)$ of the syndrome generation block is described, considering $l(X)$, as

$$\begin{aligned} s(X) &= \sum_{k=0}^{1503} s_k X^k \\ &= Q\left(\frac{l(X)[X^{1504} + X^7 + X^6 + X^4 + 1]}{X^{1504}}\right) \end{aligned} \quad (2)$$

Also, the output polynomial $f(X)$ of the FIR filtering block can be given by

$$f(X) = \sum_{k=0}^{1503} f_k X^k$$

$$= Q\left(\frac{[\sum_{i=0}^7 s_i X^i][X^8 + X^7 + X^3 + X^2 + 1]}{X^8}\right) \quad (3)$$

Note in Eq. (3) that only the last byte of the output sequence of syndrome generation block is used. Finally, the output polynomial $p(X)$ of the offset addition block, which is the parity checksum polynomial, is represented with the polynomial $f(X)$ as

$$\begin{aligned} p(X) &= \sum_{k=0}^{1503} p_k X^k \\ &= [f_7 X^7 + f_6 X^6 + \dots + f_0] + [X^6 + X^5 + X^2 + X^1 + 1] \end{aligned} \quad (4)$$

3.2 Parallel Parity Checksum Generator

The parallel processing architecture with degree eight is appropriate for parity checksum generator, because the maximum processing rate in transmission system is eight bits per clock cycle as 256 QAM is used. This parallel processing architecture would generate eight output sequences per clock cycle. For such parallel processing architecture the coefficient vectors of the polynomials in Eq. (1), Eq. (2), Eq. (3), and Eq. (4) can be treated in an eight-dimensional vector space over $GF(2)$. Let the eight coefficients of the polynomial $p(X)$ form an 8-bit binary coefficient vector $\mathbf{p} = [p_7 \ p_6 \ \dots \ p_0]^T$. The vector form expression of the coefficient vector $\mathbf{p}$ is obtained from Eq. (4)

$$\mathbf{p} = \mathbf{f} \oplus \mathbf{o} \quad (5)$$

where the coefficient vector $\mathbf{f}$ is $[f_7 \ f_6 \ \dots \ f_0]^T$ corresponding to the eight consecutive coefficients of the polynomial $f(X)$ and the coefficient vector $\mathbf{o}$ pertinent to the offset addition block is $[0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1 \ 1]^T$. The symbol $\oplus$ is the addition operator of two vectors over $GF(2)$.

The coefficient vector $\mathbf{f}$ in Eq. (5) is obtained by polynomial multiplication in Eq. (3)

$$\begin{aligned} f(X) &= s_7 X^7 + (s_7 + s_6) X^6 \\ &\quad + (s_6 + s_5) X^5 + (s_5 + s_4) X^4 \\ &\quad + (s_4 + s_3) X^3 + (s_7 + s_3 + s_2) X^2 \\ &\quad + (s_7 + s_6 + s_2 + s_1) X \\ &\quad + (s_6 + s_5 + s_1 + s_0) \end{aligned} \quad (6)$$

From Eq. (6) the coefficient vector $\mathbf{f}$ can be expressed as

$$\mathbf{f} = \mathbf{E} \otimes \mathbf{s} \quad (7)$$

where the coefficient vector $\mathbf{s}$ is composed of the eight entries of the polynomial coefficient in $s(X)$, and the matrix $\mathbf{E}$ is obtained as

$$\mathbf{E} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

from the polynomial expression of $f(X)$. The symbol $\otimes$ is the multiplication operator of a matrix with a vector or two matrices over $GF(2)$. Similarly, the coefficient vector $\mathbf{s}$ in Eq. (7) is obtained through Eq. (2) as following

$$\mathbf{s} = \mathbf{F} \oplus \mathbf{l}_0 \otimes \mathbf{l}_{187} \quad (8)$$

where the k -th coefficient vector $\mathbf{l}_k$ ($k = 0$ or 187) is $[l_{8 \cdot (187-k)+7} \ l_{8 \cdot (187-k)+6} \ \dots \ l_{8 \cdot (187-k)}]$ pertaining to the k -th byte of the output sequence of LFSR block and the matrix $\mathbf{F}$ is given as

$$\mathbf{F} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \end{bmatrix}$$

Note that only the first and the last bytes of the output sequence of LFSR block are needed to get the coefficient vector $\mathbf{s}$ in Eq. (8).

To get the coefficient vector $\mathbf{l}_k$, let $\mathbf{m}_k = [m_{8 \cdot (187-k)+7} \ m_{8 \cdot (187-k)+6} \ \dots \ m_{8 \cdot (187-k)}]$, corresponding to the k -th byte of the message sequence. Multiplying $g(X)$ with both sides of Eq. (1) leads to

$$g(X)l(X) = X^8 m(X) + R\left(\frac{X^8 m(X)}{g(X)}\right) \quad (9)$$

where the operator $R(\cdot)$ gives the remainder. The relation between $\mathbf{m}_k$ and $\mathbf{l}_k$ is given by Eq. (9) and can be expressed by a block matrix

$$\begin{bmatrix} \mathbf{G} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{H} & \mathbf{G} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{H} & \mathbf{G} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{H} & \mathbf{G} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H} & \mathbf{G} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H} & \mathbf{G} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H} & \mathbf{G} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H} & \mathbf{G} \end{bmatrix} \begin{bmatrix} \mathbf{l}_0 \\ \mathbf{l}_1 \\ \mathbf{l}_2 \\ \mathbf{l}_3 \\ \mathbf{l}_4 \\ \mathbf{l}_5 \\ \mathbf{l}_6 \\ \mathbf{l}_7 \end{bmatrix} = \begin{bmatrix} \mathbf{m}_0 \\ \mathbf{m}_1 \\ \mathbf{m}_2 \\ \mathbf{m}_3 \\ \mathbf{m}_4 \\ \mathbf{m}_5 \\ \mathbf{m}_6 \\ \mathbf{m}_7 \end{bmatrix} \quad (10)$$

where the matrices $\mathbf{G}$ and $\mathbf{H}$ involving with the generator polynomial function $g(X)$ are

$$\mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}, \quad \mathbf{H} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

The 8-by-8 matrix $\mathbf{0}$ is a zero matrix with all entries taking zero values. The vector $\mathbf{m}_{187}$ is obviously a zero vector due to the definition of the polynomial $m(X)$. The vector $\mathbf{l}_0$ is given by the first row of the block matrix in Eq. (10)

$$\mathbf{l}_0 = \mathbf{G}^{-1} \otimes \mathbf{m}_0 \quad (11)$$

where the matrix $\mathbf{G}^{-1}$ is defined as the inverse matrix of the matrix $\mathbf{G}$ and expressed as

$$\mathbf{G}^{-1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

From the block matrix expression in Eq. (10) $\mathbf{m}_1$ is given as

$$(\mathbf{H} \otimes \mathbf{l}_0) \oplus (\mathbf{G} \otimes \mathbf{l}_1) = \mathbf{m}_1 \quad (12)$$

Substituting $\mathbf{G}^{-1} \otimes \mathbf{m}_0$ in Eq. (11) for $\mathbf{l}_0$ in Eq. (12) and adding $(\mathbf{H} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}_0)$ to both sides of Eq. (12) leads to

$$(\mathbf{G} \otimes \mathbf{l}_1) = \mathbf{m}_1 \oplus (\mathbf{H} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}_0) \quad (13)$$

Multiplying $\mathbf{G}^{-1}$ for both sides of Eq. (13) results in

$$\mathbf{l}_1 = \mathbf{G}^{-1} \otimes \mathbf{m}'_1 \quad (14)$$

where the vector $\mathbf{m}'_1$ is given by

$$\mathbf{m}'_1 = \mathbf{m}_1 \oplus (\mathbf{H} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}_0).$$

Generally, the coefficient vector $\mathbf{l}_j$ ($j = 0, \dots, 187$) from Eq. (10) is given as

$$\mathbf{l}_j = \mathbf{G}^{-1} \otimes \mathbf{m}'_j \quad (15)$$

and the vector $\mathbf{m}'_j$ is obtained as following

$$\begin{aligned} \mathbf{m}'_j &= \mathbf{m}_j \oplus (\mathbf{H} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}_{j-1}), \quad j = 1, \dots, 187 \\ \mathbf{m}'_0 &= \mathbf{m}_0. \end{aligned} \quad (16)$$

By substituting the coefficient vectors obtained in Eq. (7), Eq. (8), and Eq. (15) for the coefficient vector $\mathbf{p}$ in Eq. (5), the coefficient vector $\mathbf{p}$ is represented by

$$\mathbf{p} = (\mathbf{E} \otimes \mathbf{F} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}'_0) \oplus (\mathbf{E} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}'_{187}) \quad (17)$$

Since $\mathbf{E} \otimes \mathbf{G}^{-1}$ is an 8-by-8 identity matrix due to the identity of $\mathbf{E}$ with $\mathbf{G}$, the coefficient vector $\mathbf{p}$ is simplified as

$$\mathbf{p} = (\mathbf{E} \otimes \mathbf{F} \otimes \mathbf{G}^{-1} \otimes \mathbf{m}'_0) \oplus \mathbf{m}'_{187}. \quad (18)$$

3.3 Parallel Processing Architecture for Parity Checksum Generation

From Eq. (16) and Eq. (18), the parallel processing architecture for parity checksum generation can be depicted as Fig. 4. It consists of a feedback part corresponding to the iterative operation in Eq. (16) and a feed-forward part related to the operations in Eq. (18). The functional block denoted as $\mathbf{T}_{\mathbf{H}\mathbf{G}^{-1}} \mathbf{m}'_k$ performs the matrix product of the matrix $\mathbf{T}_{\mathbf{H}\mathbf{G}^{-1}}$ and an input vector $\mathbf{m}'_k$, where $\mathbf{T}_{\mathbf{H}\mathbf{G}^{-1}}$ is given by

Fig. 4 Parallel processing architecture for parity checksum generation.

$$\mathbf{T}_{\text{HG}^{-1}} = \mathbf{H} \otimes \mathbf{G}^{-1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

The block Z^{-1} delays the input vector data by one clock cycle. In the feed-forward part, the block named $\mathbf{T}_{\text{EFG}^{-1}}\mathbf{m}'_0 + \mathbf{o}$ involves an multiplication of an input vector $\mathbf{m}'_0$ with a matrix $\mathbf{T}_{\text{EFG}^{-1}}$ and adds the coefficient vector $\mathbf{o}$. The matrix $\mathbf{T}_{\text{EFG}^{-1}}$ is given as

$$\mathbf{T}_{\text{EFG}^{-1}} = \mathbf{E} \otimes \mathbf{F} \otimes \mathbf{G}^{-1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \end{bmatrix}$$

The block $\mathbf{D}$ holds the output vector of the block $\mathbf{T}_{\text{EFG}^{-1}}\mathbf{m}'_0 + \mathbf{o}$.

For an encoding operation, the block Z^{-1} is initialized so that the memory elements contain zero values. As a result, the vector $\mathbf{m}'_0$ is equal to the vector $\mathbf{m}_0$ at the first clock cycle as indicated in Eq. (16). The feedback part performs the iterative procedure represented in Eq. (16) for the next 187 clock cycles. At 188-th clock cycle, the parity checksum is generated by adding $\mathbf{m}'_{187}$ to the vector data held in block $\mathbf{D}$.

4. Parallel Processing Architecture for Syndrome Generation

The parallel processing architecture for syndrome generation in receiver can be developed in the similar manner of parity checksum generation. Let $\bar{m}(X)$, $\bar{l}(X)$, and $\bar{s}(X)$ denote message polynomial, output polynomial of LFSR block, output polynomial in the syndrome generation block, respectively (see Fig. 3). Since the syndrome generation in receiver is affected by the previous TSP, the message polynomial $\bar{m}(X)$ is represented as

$$\bar{m}(X) = \sum_{i=0}^l (m_i(X) + p_i(X))X^{1504 \cdot (1-i)} \quad (19)$$

where $i = 0$ indicates previously received TSP and $i = 1$ corresponds to current TSP and $m_i(X)$ and $p_i(X)$ are the message polynomial and the parity checksum polynomial of the i -th TSP, respectively.

From Eq. (2) the i -th coefficient of the polynomial $\bar{s}(X)$, corresponding to the i -th syndrome bit, is given as following

$$\bar{s}_i = \bar{l}_i + \bar{l}_{i+1497} + \bar{l}_{i+1498} + \bar{l}_{i+1500} + \bar{l}_{i+1504} \quad (20)$$

where the subscript values exceeding 1503 corresponds to the output values of the LFSR block in receiver for the previous TSP. Let the eight consecutive coefficients of the polynomial $\bar{s}(X)$ form a vector $\bar{\mathbf{s}}_i = [\bar{s}_{8k} \ \bar{s}_{8k-1} \ \dots \ \bar{s}_{8k-7}]$. By Eq. (20) $\bar{s}_{8k}$ is expressed as

$$\bar{s}_{8k} = \bar{l}_{8k} + \bar{l}_{8k+1497} + \bar{l}_{8k+1498} + \bar{l}_{8k+1500} + \bar{l}_{8k+1504}$$

The subscript numbers in right hand side can be rewritten by modulo 8 expression

$$\bar{s}_{8k} = \bar{l}_{8k} + \bar{l}_{8(k+188)-7} + \bar{l}_{8(k+188)-6} + \bar{l}_{8(k+188)-4} + \bar{l}_{8(k+188)} \quad (21)$$

Likewise, remaining entries of $\bar{\mathbf{s}}_k$ can be expressed by the following equations

$$\begin{aligned} \bar{s}_{8k-1} &= \bar{l}_{8k-1} + \bar{l}_{8(k+188)} + \bar{l}_{8(k+188)-7} + \bar{l}_{8(k+188)-5} + \bar{l}_{8(k+188)-1} \\ \bar{s}_{8k-2} &= \bar{l}_{8k-2} + \bar{l}_{8(k+188)-1} + \bar{l}_{8(k+187)} + \bar{l}_{8(k+188)-6} + \bar{l}_{8(k+188)-2} \\ &\vdots \end{aligned} \quad (22)$$

$$\begin{aligned} \bar{s}_{8k-6} &= \bar{l}_{8k-6} + \bar{l}_{8(k+188)-5} + \bar{l}_{8(k+188)-4} + \bar{l}_{8(k+188)-2} + \bar{l}_{8(k+188)-6} \\ \bar{s}_{8k-7} &= \bar{l}_{8k-7} + \bar{l}_{8(k+188)-6} + \bar{l}_{8(k+188)-5} + \bar{l}_{8(k+188)-4} + \bar{l}_{8(k+188)-7} \end{aligned}$$

In vector-matrix form, the coefficient vector $\bar{\mathbf{s}}_k$ is given as follows

$$\bar{\mathbf{s}}_k = (\mathbf{V} \otimes \bar{\mathbf{l}}_{k-188}) \oplus (\mathbf{W} \otimes \bar{\mathbf{l}}_{k-187}) \oplus \bar{\mathbf{l}}_k \quad (23)$$

where the matrices $\mathbf{V}$ and $\mathbf{W}$ are expressed as

$$\mathbf{V} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \quad \mathbf{W} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \end{bmatrix}$$

Fig. 5 Parallel processing architecture for syndrome generation.

and the coefficient vector $\bar{\mathbf{l}}_k = [\bar{l}_{8k} \bar{l}_{8k-1} \dots \bar{l}_{8k-7}]$ is given by Eq. (1) as

$$\bar{\mathbf{l}}_k = \mathbf{G}^{-1} \otimes \bar{\mathbf{m}}'_k \quad (24)$$

and the vector $\bar{\mathbf{m}}'_k$ is defined as

$$\begin{aligned} \bar{\mathbf{m}}'_k &= \bar{\mathbf{m}}_k \oplus (\mathbf{H} \otimes \mathbf{G}^{-1} \otimes \bar{\mathbf{m}}'_{k-1}) \\ \bar{\mathbf{m}}'_0 &= \bar{\mathbf{m}}_0 \end{aligned} \quad (25)$$

where the vector $\bar{\mathbf{m}}_k$ is $\bar{\mathbf{m}}_k = [\bar{m}_{8k} \bar{m}_{8k-1} \dots \bar{m}_{8k-7}]$ consisting of the k -th eight consecutive coefficients in the polynomial $\bar{m}(X)$.

From Eq. (23), Eq. (24), and Eq. (25) the parallel processing architecture for syndrome generation can be depicted as Fig. 5. It consists of the feed-forward part related with Eq. (23) and feedback part involving with Eq. (24) and Eq. (25). The feedback part is identical with that of the parity checksum generator in Fig. 4, except the switch to force $\mathbf{m}_{187}$ to be a zero vector. The blocks denoted as $\mathbf{G}^{-1} \bar{\mathbf{m}}'_k$, $\mathbf{V}_{k-188}$, and $\mathbf{W}_{k-187}$ perform vector-matrix multiplication. The blocks indicated by $\mathbf{Z}^{-1}$ and $\mathbf{Z}^{-187}$ are the delay elements delaying the input vectors by 1 and 187 clock cycles, respectively.

5. Implementation Results

The proposed parallel processing architecture and the conventional serial processing architecture for the parity checksum and syndrome generation are implemented in an FPGA, EP1S25F672C6 model of Altera Corporation. Functional verification is performed by ModelSim software of Mentor Graphics Corporation.

Table 1 shows the compilation results in terms of hardware complexity, processing time, and power consumption. The number of logic cells represents the hardware complexity and the minimum clock period, which is an inverse of maximum clock frequency, indicates the operating speed of

Table 1 Comparisons of implementation results.

Architectures	Parity checksum generator		Syndrome generator	
	Serial [1]	Parallel	Serial [1]	Parallel
Logic cells	1554	50	1512	1542
Minimum clock period (nanosecond)	8.10	5.50	2.53	3.82
Processing time (nanosecond)	12182	1034	3805	720
Power dissipation (mW)	8.12 @16MHz	0.02 @2MHz	3.35 @16MHz	0.43 @2MHz

the circuit [10]. The processing time is computed by multiplying the minimum clock period with the number of the clocks required to process a TSP. For a comparison of power consumption, we considered that both architectures have the same processing speed, specifically 10.6 K TPS per second, i.e. 16 Mbps. This processing speed is obtained by setting the clock frequency at 16 MHz for the serial architectures and 2 MHz for the parallel architecture.

In case of parity checksum generation the proposed parallel architecture requires much fewer logic cells than the serial architecture due to removing the 1497 registers used for the input of the syndrome generation block. The minimum clock period of the parallel architecture is reduced because of the simplified logic circuit including much smaller combinational logic for the switch controlled by 8-bit counter, i.e., counting up to 187, whereas serial processing architecture needs considerable size of combinational logic to control 11-bit counter counting up to 1503. The parallel architecture for syndrome generation takes a little more logic cells and requires larger minimum clock period than the serial architecture, due to byte-wise operation of the parallel architecture. Implementation results show that the proposed parallel architecture reduces the logic cells by 97% for the parity checksum generation and increases those by 2% for the syndrome generation.

The proposed parallel processing architecture significantly reduces the processing time. The processing time is obtained by multiplying the minimum clock period with 1504 bits for serial processing architecture and 188 bytes for parallel processing architecture. As a result, proposed parallel architecture reduces the processing time for a TSP by 92% for parity checksum generation and 81% for syndrome generation.

The proposed parallel processing architectures generate the parity checksum and syndrome with much lower power consumption over the serial processing architectures. It is achieved by reducing the clock frequency of the parallel architecture by one-eighth over that of the serial architectures. Moreover, for parity checksum generation, much fewer logic cells also contribute to the significant power reduction. The implementation results show that the parallel architectures reduce the power consumption by 99% for parity checksum generation and 87% for syndrome generation

over the serial architecture, respectively.

6. Conclusions

A new parallel processing architecture to remove the performance bottleneck that occurs in the transmission of digital video and audio signals over coaxial cables is proposed in this paper. The parallel processing architecture complies with ITU-T J.83 Annex B standard. Implementation results demonstrate that the proposed parallel processing architecture significantly reduces the processing time without incurring additional hardware resource.

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