Negation-Limited Inverters of Linear Size

Hiroki MORIZUMI^{†a)}, Member and Genki SUZUKI^{††}, Nonmember

SUMMARY An inverter is a circuit which outputs $\neg x_1, \neg x_2, \dots, \neg x_n$ for any Boolean inputs $x_1, x_2, \dots, x_n$. We consider constructing an inverter with AND gates and OR gates and a few NOT gates. Beals, Nishino and Tanaka have given a construction of an inverter which has size $O(n \log n)$ and depth $O(\log n)$ and uses $\lceil \log(n+1) \rceil$ NOT gates. In this paper we give a construction of an inverter which has size $O(n)$ and depth $\log^{1+o(1)} n$ and uses $\log^{1+o(1)} n$ NOT gates. This is the first negation-limited inverter of linear size using only $o(n)$ NOT gates. We also discuss implications of our construction for negation-limited circuit complexity.

key words: circuit complexity, negation-limited circuit, inverter, NOT gate

1. Introduction

No superlinear lower bound has been known so far on the size of Boolean circuits computing an explicit Boolean function, while exponential lower bounds have been known on the size of *monotone* circuits, which consist of only AND and OR gates and do not include NOT gates [2], [5], [16]. It is natural to ask: what happens if a limited number of NOT gates are allowed? This motivates us to study the *negation-limited* circuit complexity under various scenarios [3], [4], [6], [10], [17], [20].

An *inverter* is a circuit which outputs $\neg x_1, \neg x_2, \dots, \neg x_n$ for any n Boolean inputs $x_1, x_2, \dots, x_n$. One can easily construct an inverter by placing n NOT gates in a row. We wish to construct an inverter by using fewer than n NOT gates and an arbitrary number of AND gates and OR gates. It is known that $\lceil \log(n+1) \rceil$ NOT gates are necessary and sufficient to construct an inverter [13]. (All logarithms in the paper are base 2.) After constructions by Fischer [7], [8] and by Tanaka and Nishino [22], Beals, Nishino and Tanaka constructed an inverter of size $O(n \log n)$ and depth $O(\log n)$ using $\lceil \log(n+1) \rceil$ NOT gates [6]. All these constructions include only $\lceil \log(n+1) \rceil$ NOT gates, and however have nonlinear size. In the paper, we consider constructing an inverter of linear size with a few NOT gates. No inverter of linear size was known even for the case where the number of NOT gates is $o(n)$. We give a construction of an inverter which has size $O(n)$ and depth $\log^{1+o(1)} n$ and uses $\log^{1+o(1)} n$ NOT gates. The results are summarized in Table. 1.

It is known that a construction of a negation-limited

Table 1 Negation-limited inverters.

	# of NOTs	size	depth
trivial	n	n	1
this paper	$\log^{1+o(1)} n$	$O(n)$	$\log^{1+o(1)} n$
[6]	$\lceil \log(n+1) \rceil$	$O(n \log n)$	$O(\log n)$

inverter implies a relation between negation-limited circuits and *general* circuits, which are circuits with no limitation of the number of NOT gates, for these sizes. More precisely, if there are a general circuit of size s_1 computing an arbitrary Boolean function f and an inverter of size s_2 with r NOT gates, then there is a circuit of size $2s_1 + s_2$ with at most r NOT gates computing f . In the paper, we give such a relation which is implied by our construction of inverters, and discuss two implications of the relation.

2. Preliminaries

In the paper, a *circuit* is an acyclic Boolean circuit which consists of AND gates of fan-in two, OR gates of fan-in two and NOT gates. The *size* of a circuit C is the number of gates in C , and denoted by $\text{size}(C)$. The *depth* of C is the length (number of gates) of the longest path in C , and denoted by $\text{depth}(C)$. We denote by $\text{not}(C)$ the number of NOT gates in C .

The function $\log^{(i)} x$ is defined recursively for nonnegative integers i and real numbers x as follows:

$$\log^{(i)} x = \begin{cases} x & \text{if } i = 0; \\ \log(\log^{(i-1)} x) & \text{if } i > 0 \text{ and } \log^{(i-1)} x > 0; \\ \text{undefined} & \text{otherwise.} \end{cases}$$

The iterated logarithm function $\log^* x$ is defined as follows:

$$\log^* x = \min \{i \geq 0 : \log^{(i)} x \leq 1\}.$$

In our construction, we use the following negation-limited inverter.

Proposition 1: (Beals, Nishino and Tanaka [6]) There is an inverter of size $O(n \log n)$ and depth $O(\log n)$ using $\lceil \log(n+1) \rceil$ NOT gates.

3. Negation-Limited Inverter

In this section, we construct an inverter of size $O(n)$ and depth $\log^{1+o(1)} n$ using $\log^{1+o(1)} n$ NOT gates.

Manuscript received March 2, 2009.

Manuscript revised June 30, 2009.

[†]The author is with the Graduate School of Information Sciences, Tohoku University, Sendai-shi, 980-8579 Japan.

^{††}The author is with the School of Engineering, Tohoku University, Sendai-shi, 980-8579 Japan.

a) E-mail: morizumi@ecei.tohoku.ac.jp

DOI: 10.1587/transinf.E93.D.257

Fig. 1 Overall structure of the inverter I' .

3.3 Proof of Lemma 1

Proof of Lemma 1. We give a construction of the inverter I' in Lemma 1. We can assume that n is enough large since we choose some enough large constant as n_0 in Lemma 1.

See Fig. 1. We first partition n inputs $x_1, x_2, \dots, x_n$ of the inverter I' to $n_b = \lceil n / (3 \lceil \log^{(i)} n \rceil) \rceil$ blocks so that each block contains $n_i = 3 \lceil \log^{(i)} n \rceil$ inputs. If necessary, we pad the last block with constants 0's so that the block contains exactly n_i inputs. For the k -th block of inputs, $1 \leq k \leq n_b$, we construct an inverter C^k for the inputs in the block. As C^k we use the inverter in Proposition 1. We choose the constant c_0 in Lemma 1 so that the n_i -input inverter of Proposition 1 exists. The input of C^k are $x_{n_i(k-1)+1}, \dots, x_{n_i k}$ where for each $l > n$, x_l is replaced to 0. C^k is represented by a rectangle of solid lines in Fig. 1. The set of inverters $C^1, C^2, \dots, C^{n_b}$ forms an inverter for $x_1, x_2, \dots, x_n$. By Proposition 1, for $1 \leq k \leq n_b$, the size and the depth of each C^k are as follows.

$$\text{size}(C^k) \leq c_s n_i \log n_i. \quad (2)$$

$$\text{depth}(C^k) \leq c_d \log n_i. \quad (3)$$

Next we replace NOT gates in C^k 's to several inverters as follows. By Proposition 1, each C^k includes $\lceil \log(n_i + 1) \rceil$ NOT gates. Let N_j^k be the j -th NOT gate from the input side in C^k for $1 \leq j \leq \lceil \log(n_i + 1) \rceil$ and $1 \leq k \leq n_b$. More precisely, we choose each number j so that there is no path from the output of N_j^k to the input of $N_{j'}^k$ if $j' \leq j$. For each j , we replace n_b NOT gates $N_j^1, N_j^2, \dots, N_j^{n_b}$ to one n_b -input inverter C'_j . C'_j is represented by a rectangle of broken

lines in Fig. 1. As C'_j we use the inverter I in Lemma 1. The n_b -input inverter I exists, since $n_b = \lceil n / (3 \lceil \log^{(i)} n \rceil) \rceil \geq n / (4 \log n)$.

The construction of the inverter I' has been completed. If the replacements of NOT gates to C'_j 's induce a loop through some C'_j 's, then I' may not behave as an inverter. However, we can prove that there is no loop in I' by the following way. We assume that there is a loop in I' and show a contradiction. Let l be a loop in I' . Since all C^k 's, $1 \leq k \leq n_b$, before replacement have no loop, l must be through some C'_j 's, $1 \leq j \leq \lceil \log(n_i + 1) \rceil$. Let $C'_{j_1}, C'_{j_2}, \dots, C'_{j_p}$ be all C'_j 's which l is through in the order. After C'_{j_p} , l goes to C'_{j_1} , since l is a loop. Since there is no path from the output of $N_{j_1}^k$ to the input of $N_{j_2}^k$ if $j_2 \leq j_1$, $j_2 < j_1$ for $1 \leq i \leq p-1$, and $j_p < j_1$. Thus a contradiction happens.

In the rest, we confirm that the circuit I' satisfies the condition of the size, the depth and the number of NOT gates. The size, the depth and the number of NOT gates of I' are obtained from the ones of C^k 's and C'_j 's. We have already shown $\text{size}(C^k)$ and $\text{depth}(C^k)$ in Eq. (2) and Eq. (3), respectively. We do not have to consider $\text{not}(C^k)$ since all NOT gates in C^k 's have been replaced to C'_j 's. By the condition of I in Lemma 1, for $1 \leq j \leq \lceil \log(n_i + 1) \rceil$, the size, the depth and the number of NOT gates of each C'_j are as follows.

$$\text{size}(C'_j) \leq 2c_s n_b \log^{(i)} n_b. \quad (4)$$

$$\text{depth}(C'_j) \leq c_d (\log^{[i-1]} n_b) (\log^{(i)} n_b + 4). \quad (5)$$

Fig. 2 The conversion from a general circuit to a negation-limited circuit.

$$\text{not}(C'_j) \leq (\log^{[i-1]} n_b)(\log^{(i)} n_b + 4). \quad (6)$$

By Eq. (2) to Eq. (6), the size, the depth and the number of NOT gates of I' are as follows. In the following, we use the assumption that n is enough large.

$$\begin{aligned} \text{size}(I') &\leq n_b \cdot \text{size}(C^k) + \lceil \log(n_i + 1) \rceil \cdot \text{size}(C'_j) \\ &\leq n_b \cdot c_s n_i \log n_i + \lceil \log(n_i + 1) \rceil \cdot 2c_s n_b \log^{(i)} n_b \\ &\leq c_s n_b (n_i + 2 \log^{(i)} n_b) \lceil \log(n_i + 1) \rceil \\ &\leq c_s (\lceil n / (3 \lceil \log^{(i)} n \rceil) \rceil) (3 \lceil \log^{(i)} n \rceil + 2 \log^{(i)} n) \\ &\quad \cdot \lceil \log(3 \lceil \log^{(i)} n \rceil + 1) \rceil \\ &\leq c_s ((n / 3 \log^{(i)} n) + 1) (5 \log^{(i)} n + 3) (\log^{(i+1)} n + 3) \\ &\leq c_s (11/6) n (\log^{(i+1)} n + 3) \\ &\leq 2c_s n \log^{(i+1)} n. \end{aligned}$$

$$\begin{aligned} \text{depth}(I') &\leq \text{depth}(C^k) + \lceil \log(n_i + 1) \rceil \cdot \text{depth}(C'_j) \\ &\leq c_d \log n_i \\ &\quad + \lceil \log(n_i + 1) \rceil \cdot c_d (\log^{[i-1]} n_b) (\log^{(i)} n_b + 4) \\ &\leq c_d \log n_i \\ &\quad + c_d (\log^{[i-1]} n) (\log^{(i)} n + 4) \lceil \log(3 \lceil \log^{(i)} n \rceil + 1) \rceil \\ &\leq c_d (\log^{[i-1]} n) (\log^{(i)} n + 4) (\log^{(i+1)} n + 3) \\ &\leq c_d (\log^{[i-1]} n) (\log^{(i)} n) (\log^{(i+1)} n + 4) \\ &= c_d (\log^{[i]} n) (\log^{(i+1)} n + 4). \end{aligned}$$

$$\begin{aligned} \text{not}(I') &\leq \lceil \log(n_i + 1) \rceil \cdot \text{not}(C'_j) \\ &\leq \lceil \log(n_i + 1) \rceil \cdot (\log^{[i-1]} n_b) (\log^{(i)} n_b + 4) \\ &\leq (\log^{[i-1]} n) (\log^{(i)} n + 4) \cdot \lceil \log(3 \lceil \log^{(i)} n \rceil + 1) \rceil \\ &\leq (\log^{[i-1]} n) (\log^{(i)} n + 4) (\log^{(i+1)} n + 3) \end{aligned}$$

$$\begin{aligned} &\leq (\log^{[i-1]} n) (\log^{(i)} n) (\log^{(i+1)} n + 4) \\ &= (\log^{[i]} n) (\log^{(i+1)} n + 4). \end{aligned}$$

□

As proved above, the constructed circuit I' has no loop, which is guaranteed by replacing NOT gates $N_j^1, N_j^2, \dots, N_j^{n_b}$ to one inverter C'_j for each j . If we replace NOT gates including two NOT gates $N_{j_1}^k$ and $N_{j_2}^k$ for some k to one inverter, the obtained circuit has a loop.

4. General Circuits and Negation-Limited Circuits

In this section, we give a relation between general circuits and negation-limited circuits for these sizes and discuss two implications of the relation. We denote by $\text{size}(f)$ the size of the smallest circuit computing a function f and denote by $\text{size}_r(f)$ the size of the smallest circuit with at most r NOT gates computing f . f can be a multi-output function.

See Fig. 2. Let C be a general circuit computing an arbitrary Boolean function f . The well-known technique based on DeMorgan's laws can move all NOT gates in the circuit C to the inputs side with at most twice increase of the size. If we use an inverter with r NOT gates to obtain $\neg x_1, \neg x_2, \dots, \neg x_n$, the overall circuit includes only r NOT gates. Beals, Nishino and Tanaka used the inverter of Proposition 1 in the conversion of circuits and obtained the following corollary:

Corollary 1: (Beals, Nishino and Tanaka [6]) For every function f ,

$$\text{size}_{\lceil \log(n+1) \rceil}(f) \leq 2\text{size}(f) + O(n \log n).$$

Our construction gives the following corollary:

Corollary 2: For every function f ,

$$\text{size}_{\log^{1+o(1)} n}(f) \leq 2\text{size}(f) + O(n).$$

$O(n \log n)$ in Corollary 1 and $O(n)$ in Corollary 2 are the size of the inverter which is used in each conversion.

Corollary 2 is useful to prove upper bounds on the size for negation-limited circuits computing some functions. Consider sorters for example. A *sorter* is a circuit which sorts the inputs $x_1, x_2, \dots, x_n$, i.e., outputs $y_1, y_2, \dots, y_n$ such that $y_1 \geq y_2 \geq \dots \geq y_n$ and $\Sigma x_i = \Sigma y_i$. Negation-limited sorters or circuits computing the merging function, which can be regarded as restricted sorters, have been studied in several papers [4], [14], [18]. Although if the number of NOT gates is not limited, then there is a sorter of size $O(n)$ (Theorem 4.1 in p. 76 of [24]), it was not known whether there is a sorter of size $O(n)$ using $o(n)$ NOT gates. Corollary 2 immediately gives the following theorem:

Theorem 2: There is a sorter of size $O(n)$ using $\log^{1+o(1)} n$ NOT gates.

Although by Corollary 1 we can prove that there is a sorter of size $O(n \log n)$ using $\lceil \log(n+1) \rceil$ NOT gates, it has been known that a sorter of size $O(n \log n)$ exists even if NOT gates are not allowed to use [1].

Another implication of Corollary 2 is an approach to prove a superlinear size lower bound for general circuits. To prove a superlinear lower bound on the size of general circuits computing an explicit function is one of the most challenging open problems in computational complexity theory. By Corollary 2, when one tries to prove a superlinear size lower bound for general circuits, it is enough to prove a superlinear size lower bound for circuits using at most $\log^{1+o(1)} n$ NOT gates. At the case of Corollary 1, an $\omega(n \log n)$ size lower bound for circuits using at most $\lceil \log(n+1) \rceil$ NOT gates is needed. This difference between superlinear and $\omega(n \log n)$ lower bounds may be meaningful, since $\Omega(n \log n)$ lower bounds are known for some n -input n -output functions [11], [12], [15], although the lower bounds are only for monotone circuits. Even for n -output functions, no superlinear size lower bound for general circuits have been known.

5. Concluding Remarks and Open Problems

The following question by Turán is known as an open problem [6]: is the size of any inverter with $O(\log n)$ NOT gates and $O(\log n)$ depth superlinear? The known results related to Turán's question are summarized as follows. The results on a construction of a negation-limited inverter have been presented in Table 1 of Section 1. The best known lower bound on the size of negation-limited inverters is linear even for the case where the number of NOT gates is limited to $\log(n+1)$ [9]. Turán's question has been solved if we restrict inputs as follows. A binary sequence $x_1, x_2, \dots, x_n$ is k -tonic for a positive integer k , $1 \leq k \leq n-1$, if the number of i 's, $1 \leq i \leq n-1$, such that $x_i \neq x_{i+1}$ is at most k . A circuit inverting k -tonic sequences can be constructed with size $O(n)$ and depth $O(\log n)$ and $O(\log n)$ NOT gates for the

case where $k = O(1)$ [14], [18], which means that if inputs are restricted to $O(1)$ -tonic sequences, then the answer of Turán's question is "no". In this paper we gave a construction of an inverter of size $O(n)$ and depth $\log^{1+o(1)} n$ using $\log^{1+o(1)} n$ NOT gates. Our construction means that one can construct an inverter of linear size if one can use a little more than $O(\log n)$ NOT gates and the depth can be a little bigger than $O(\log n)$.

A natural next step towards a solution of Turán's question is reducing the number of NOT gates to $O(\log n)$ or the depth to $O(\log n)$. Our construction has a recursive structure. Although we may be able to improve the number of NOT gates or the depth to a smaller number than Theorem 1 by a similar recursive structure, it is difficult to reduce it to $O(\log n)$. To achieve $O(\log n)$, another construction is needed.

Acknowledgments

We would like to sincerely thank Professor Takao Nishizeki who read the early version of this paper and gave us valuable comments and suggestions.

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Hiroki Morizumi received the B.E., M.I., and Ph.D. degrees in informatics from Kyoto University, Kyoto, Japan in 2002, 2004 and 2007, respectively. He is currently an assistant professor of Graduate School of Information Sciences, Tohoku University, Sendai, Japan. His research interests include complexity theory and algorithms.

Genki Suzuki received the B.E. degree from Tohoku University, Sendai, Japan in 2008. He is currently a student of Graduate School of Engineering, Tohoku University, Sendai, Japan.