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Development and Outdoor Evaluation of an Experimental Platform in an 80-MHz Bandwidth 2×2 MIMO-OFDM System in 5.2-GHz Band

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SUMMARY The IEEE802.11ac task group has announced the use of a wider channel that extends the channel bandwidth to more than 80 MHz. We present an experimental platform consisting of a baseband and a RF unit in a 2×2 MIMO-OFDM system for the wider channel and report its system performance results from a field experiment. The MIMO-OFDM transceiver in the baseband unit has been designed to detect real-time MIMO and provides a maximum data rate of 600 Mbps. OFDM tends to cause high peak PAPR for wider channels and distorts the power amplifier performance in the RF unit. We have improved the non-linear distortion by optimizing the OFDM preamble and evaluated its performance by conducting a simulation integrated with baseband processing and a RF. In the field experiment, our platform tested the communication performance in a farm and a passage environment.

key words: IEEE802.11ac, wideband MIMO-OFDM, FPGA, field experiment

1. Introduction

A multiple-input multiple-output (MIMO) technique is commonly used to improve the communication reliability or increase the data throughput by using spatial division multiplexing (SDM). Orthogonal division frequency multiplexing (OFDM) has been known as a powerful technique for equalizing the received signals in multipath fading environments. A MIMO-OFDM system, which is a combination of these techniques, has attracted a great deal of attention in current wireless communications. The IEEE802.11n standard supports MIMO-OFDM in a mandatory mode. The IEEE802.11ac task group (TG) for the next-generation WLAN standard targets a throughput of over 1 Gbps in the MAC layer [1], [2]. Multi-user MIMO is a key technology for enhancing the space utilization efficiency in limited frequency bands. In addition to multi-user MIMO, a wider channel, which extends the channel bandwidth to more than 80 MHz, will be supported to ensure higher data rates.

While the performance achievement of MIMO-OFDM has been proven in theoretical modeling and using numerical simulations, its hardware development still remains a

challenging issue. A large testbed for super 3G and IMT-Advanced systems has been used for the MIMO propagation measurements in [3], [4]. These testbeds assume the position of the wireless base stations and are not for mobile user terminals. In general, a small wireless terminal is developed by integrating the baseband and radio frequency (RF) transceiver LSIs. An application-specific integrated circuit (ASIC) is desirable due to their low power consumption, where VLSI implementation of a 4×4 MIMO-OFDM baseband transceiver with a data rate of 192 Mbps has been presented in [5]. In our previous work, we designed 2×2 and 4×4 MIMO-OFDM baseband transceiver LSIs [6], [7], which provide maximum data rates of 600 Mbps and 1.5 Gbps in the 80-MHz channel, respectively. A field-programmable gate array (FPGA) is a reconfigurable logic device that can be configured by the users after manufacturing. FPGAs are preferred to ASICs for prototyping experimental platforms. Several studies [8], [9] have implemented their proposed algorithms into FPGAs.

Our research group aims to develop a wireless video transmission system to meet the outdoor usage model outlined in the IEEE802.11ac TG [1]. A wider channel of more than 80 MHz was created in our previous design [6]. Our continued work is to develop an experimental platform integrated with baseband and RF units. There are several studies about a total platform design that integrates both the baseband and RF units in MIMO-OFDM and enables testing in a field experiment. Even recent studies [8], [9] deal with only a FPGA implementation in a baseband MIMO-OFDM transceiver. Jungnickel et al. has reported the total development of a MIMO-OFDM experimental platform [10]. We compare Jungnickel's experimental platform with ours, which is summarized in Table 1. The wireless specifications (MIMO-OFDM, RF carrier frequency, bandwidth, etc) of the two experimental platforms are relatively similar. However, there is a large difference between the MIMO computation times and communication environments. Jungnickel's platform takes 500 μ s for the MIMO computation, which cannot perform both the MIMO channel computation and detection (using the results from its computation) on the same frame. This shows that Jungnickel's platform is not suitable for time-variant channels under fast fading. On the other hand, our platform is based on dedicated hardware and speeds up the MIMO channel computation about

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Table 1 Comparison of experimental platforms.

	Ref. [10]	Our Work
System	SISO-OFDM 2x2/3x3/3x5 MIMO-OFDM	2x2 MIMO-OFDM
RF Carrier Frequency	5.26 GHz	5.2 GHz
Bandwidth (Including Guard Band)	100 MHz	100 MHz
Occupied Signal Bandwidth	75 MHz	80 MHz
Baseband Transceiver Implementation	FPGA & DSP	FPGA
RF Transceiver	Dual-Stage Up-Conversion (900-MHz IF)	Dual-Stage Up-Conversion (374-MHz IF)
Maximum Transmit Power per Antenna	0 dBm	24 dBm
OFDM Subcarrier Count	64 (48 Data Subcarriers)	512 (408 Data Subcarriers)
MIMO Channel Computation Time	500 μ s	0.19 μ s
Adaptation to Time- Variant Channel	Slow Fading	Fast Fading
Communication Environment	Indoor	Outdoor
Experimental Place	Office Room (15 x 7 x 2.80 m ³)	Passage (160 x 5 m ²) Farm (160 x 5 m ²)
Measurement Distance	4 m	10 to 160 m

2,500 times. Moreover, our platform is designed to communicate in outdoor environments. We have fabricated a new RF transceiver with a maximum transmit power of 24 dBm to extend the communication distance. Existing RF transceivers cannot meet our targeting performance. For instance, a typical RF transceiver in IEEE802.11n supports a 40-MHz bandwidth and a transmit power of about 17 dBm. We started by optimizing the RF parameters through the use of a baseband-RF simulation and tested the fabricated RF transceiver. To the best of our knowledge, our work is the first to try to develop an experimental platform assuming the IEEE802.11ac outdoor usage model.

2. MIMO-OFDM Transceiver

Figure 1 shows a block diagram of a 2x2 MIMO-OFDM transceiver. The functions in the transmitter and receiver blocks are the same as those of IEEE802.11n PHY. The MIMO detection is used to recover the data symbols from spatially multiplexed data streams. We have taken into consideration a new frame format for the wider 80-MHz channel. The OFDM parameters are enumerated in Table 2. Based on a 512-point FFT/IFFT, this specification reaches a maximum 600 Mbps and 1.5 Gbps for the data rates in the 2x2 and 4x4 MIMO, respectively. We have designed digital signal processing circuits according to the block diagram. In the FFT/IFFT block, a pipeline FFT based on a Radix-2 and a Radix-2² single-path delay feedback (R2SDF and R2²SDF) hybrid architecture [11] is implemented, whose structure is shown in Fig. 2. It enables for high-speed computation and efficient memory utilization by using a low-speed clock whose clock frequency corresponds to the baseband sampling rate. The Viterbi decoder is illustrated in

Fig. 1 Block diagram of 2x2 MIMO-OFDM transceiver.**Table 2** OFDM parameters for 80-MHz bandwidth MIMO-OFDM.

Channel bandwidth	80 MHz
Number of FFT/IFFT points	512
Subcarrier frequency spacing	0.1563 MHz
Number of data subcarriers	480
Preamble duration	16 μ s
Symbol duration	7.2 μ s
FFT/IFFT window duration	6.4 μ s
Guard interval duration	0.4 μ s, 0.8 μ s
Supported modulation modes	QPSK, 16QAM, 64QAM
Supported coding rates	1/2, 3/4, 5/6
Maximum Data Rate(PHY)	600Mbps (2x2 MIMO) 1.5GHz (4x4 MIMO)

Fig. 2 Circuit structure in FFT/IFFT block. **Fig. 3** Circuit structure in Viterbi decoder block.

Fig. 3. It consists of an add compare selector (ACS), a survivor path memory (SVPM), and a trace back unit (TBU). We have adopted a radix-4 architecture [12] to increase the degree of parallelism.

The frame structure, a block diagram, and the processing timing in the MIMO detection block are illustrated in Fig. 4. The MIMO frame consists of a short symbol, long training symbols, and data symbols. The long training sym-

Fig. 4 Frame structure, block diagram, and processing timing in MIMO detection.

Fig. 5 Circuit structure in MMSE algorithm.

bols $T[k]$ are used for estimating the MIMO channel matrix $H[k]$. Each element in the training symbols is expressed as $T_{ij}[k]$ with a i -th symbol index, a j -th stream, and a k -th subcarrier index. When receiving the long training symbols, the MIMO detection block performs a channel estimation and a matrix inversion given by $G[k] = H[k]^{-1}$ (called “pre-processing”) on a subcarrier-by-subcarrier basis. When receiving the $D[k]$ data symbols, the MIMO block recovers the transmitted data symbols by using $y_i[k] = G[k] D_i[k]$. If the total processing delay caused by the channel estimation and the pre-processing is shorter than the guard interval time length, the MIMO detection can achieve a real-time operation (“**Latency**” in Fig. 4). A zero-forcing (ZF) algorithm simply inverts the channel matrix H . A QR decomposition is commonly used to reduce any complexity. However, the complexity for a 2×2 matrix is not much different from an analytic solution. Figure 5 shows the circuit structure in the MMSE algorithm, which adds a noise interference component given by σ^2 . This circuit has 12 pipeline stages including an 8-stage complex division and performs the pipeline processing on a subcarrier-by-subcarrier basis. It enables the processing of a block of data for all the subcarriers and provides a constant latency time independent of the number of subcarriers. The detailed architecture of a 2×2 matrix inversion has been presented in [6]. The total latency is 15 cycles including the memory access. The latency time is 187.5 ns at a clock frequency of 80 MHz. Since the latency

Table 3 FPGA synthesis results from 2×2 MIMO-OFDM transceiver.

Preamble		LUTs	Registers
	Preamble ROM	656	75
Transmitter		LUTs	Registers
	IFFT Processor	8,236	1,804
	Others	5,220	1,817
	TX Total	13,456	3,621
Receiver		LUTs	Registers
	FFT Processor	14,848	2,204
	MIMO Decoder	14,319	2,271
	Viterbi Decoder	15,010	3,948
	Others	7,618	3,458
	RX Total	51,858	11,881
Total (Percentage in FPGA Utilization)		65,970 (31.8 %)	15,577 (7.5 %)

time is shorter than the guard intervals of 400 and 800 ns defined in the IEEE802.11n frame format, our transceiver can provide real-time operations. Moreover, the guard interval could also be shorter according to an actual measurement in a maximum delay spread. According to our measurement, the maximum delay spread was 260 ns (Sect. 4.2).

Table 3 presents the FPGA synthesis results in from the 2×2 MIMO-OFDM transceiver, where we use a Xilinx Virtex-5 XC5VLX330T FPGA device. The 2×2 MIMO-OFDM transceiver has 14 bits in the input/output ports with a maximum 20 bits in the arithmetic operations. The result of a maximum clock frequency is 108 MHz. The utilization of LUTs and registers are summarized to evaluate a circuit scale. The total percentage of FPGA utilization is at most about 32% at most. The transceiver can be implemented into the target device with the other peripheral circuits (mentioned in Sect. 3.2). The FFT/IFFT processor, the Viterbi decoder, and the MIMO decoder are dominant in the FPGA utilization.

3. Experimental Platform

3.1 Structure

The experimental platform we developed is illustrated in Fig. 6. The baseband unit consists of the FPGA and CPU boards. In the CPU board, an embedded PC provides the monitor display and network connection. The FPGA board is controlled by the commands sent from the CPU board. We have developed a GUI-based measurement software on this computer platform to evaluate the communication performance and propagation channel characteristics during the field experiment. The measurement software provides the signals monitoring and bit error rate (BER), packet error rate (PER), and QAM constellation measurements. The baseband signals in the FPGA board are inputted into the DAC modules and outputted from the ADC modules. The RF unit is designed based on super heterodyne architecture where the signals are modulated/demodulated at 5200 MHz and

Fig. 6 Experimental platform.

374 MHz in the RF and intermediate frequency (IF) bands, respectively.

3.2 FPGA Board

A block diagram of the FPGA board is illustrated in Fig. 7. The transmitted data sent from the CPU board are encoded and converted into MIMO-OFDM signals in the “Data Encoding” and “MIMO-OFDM transmitter”, respectively. The “Up sampling” block performs the low-pass filtering. The DAC and ADC modules operate at 200 MHz using double-data-rate (DDR) transfers, which corresponds to the 400-Msps data sampling rate. We use a 100-MHz clock in the MIMO-OFDM transceiver so that the 100-Msps baseband signals are up-sampled by a factor of four. According to the shifting from 80 to 100 MHz in the baseband sampling rate, we have changed the number of data subcarriers from 480 to 408 (Table 2).

The signals in the up-sampling unit are interpolated and filtered by the low-pass FIR filter. The circuit structure of the designed FIR filter of 64 orders is shown in Fig. 8. Since FPGAs have a lower circuit speed than ASICs, it is difficult to use a 400-MHz high-speed clock to correspond to the 400-Msps ADC/DAC sampling speed. We have adopted a polyphase structure where the four outputs of $y(t)$, $y(t+1)$, $y(t+2)$, and $y(t+3)$ are concurrently computed. This allows

Fig. 7 Block diagram of FPGA board.

Fig. 8 Circuit structure of low-pass FIR filter.

Fig. 9 Multiplier-based and CSD representation structures.

for a single 100-MHz clock operation. The output data are fed to the DAC modules by changing the data transfer architecture. Four parallel data at 100 MHz are converted into 200-MHz double data rate (DDR) twist pair lines. In order to reduce the FPGA resource utilization, we have adopted a canonic signed digit (CSD) representation [13] in the FIR filter implementation. Figure 9 shows the multiplier-based and CSD representation structures. The CSD representation structure replaces the multiplication by a constant value in the FIR filter coefficient with left-shift operations and additions. The implementation results are presented in Table 4. The DSP block, which is called “DSP48E” in the Xilinx Virtex-5 FPGA, consists of a multiplier, multiplier-accumulator, multiplier-adder/subtractor, and registers. It provides a faster circuit speed and less resource utilization than basic LUTs and registers. However, the number of DSP blocks is limited. The multiplier-based structure lacks the

Table 4 FIR filter implementation results.

	CSD Representation	Multiplier (DSP Blocks)	Multiplier (LUTs)
LUTs (Utilization Ratio)	11,328 (5.5 %)	1,152 (0.4 %)	53,888 (26.0 %)
Registers (Utilization Ratio)	6,952 (2.5 %)	1,204 (0.5 %)	16,176 (7.8 %)
DSP48Es (Utilization Ratio)	0 (0 %)	256 (133.3 %)	0 (0 %)
Maximum Clock Speed	159.6 MHz	167.4 MHz	68.1 MHz

Fig. 10 Power spectrum with/without low-pass FIR filter.

necessary DSP blocks even for the largest FPGA device of XC5VLX330T. When the multiplier-based structure is implemented by the LUTs and registers, its clock speed does not satisfy the 100-MHz clock requirement. The CSD representation structure decreases the clock speed slightly more than the multiplier-based structure implemented by the DSP blocks. However, it satisfies all the conditions in the FPGA resource utilization. The number of LUTs and registers here is considerably reduced compared with the multiplier-based structure. Since the CSD representation structure does not rely on specific FPGA components such as the intellectual property (IP) building blocks, it is also possible to implement it in CMOS standard cells.

The power spectrum of the up-sampled signals with/without the low-pass filter is illustrated in Fig. 10. The unnecessary side-robe is reduced by more than 30 dB_r due to the use of the low-pass filter. The shape of the power spectrum with a 100-MHz bandwidth can satisfy the regulated spectrum mask in the 5150–5250 MHz band.

3.3 RF Transceiver

3.3.1 OFDM Preamble

OFDM is known for generating a high peak-to-average power ratio (PAPR) in modulated signals. The number of OFDM subcarriers increases by extending the signal bandwidth. An OFDM transceiver with an 80-MHz bandwidth has a higher PAPR than the existing OFDM systems with 20- or 40-MHz bandwidths. The peak part of signals exceeding the output bound of the power amplifier is clipped and flattened when the amplifier operates in a nonlinear region, which causes spectrum radiation. These affected signals would be difficult to correctly demodulate on a receiver. We have optimized the OFDM preambles to reduce the PAPRs. Figure 11 shows the preamble signals for two types

(a) Preamble A

(b) Preamble B

Fig. 11 Preamble signals.**Table 5** Simulation conditions.

RMS Delay Spread	50 ns
Channel Model	HIPERLAN/2 Channel A
Doppler Frequency	50 Hz
Packet Count	2,000
Number of OFDM Symbols	8
Modulation Method	QPSK, 16QAM, 64QAM
Encoding Rate	$R = 1/2, 2/3, 3/4$
Decoding Method	Soft-Decision Viterbi Decoding

of preambles used in the long training symbols. “Preamble A” has been designed by extending the subcarrier assignments in IEEE802.11a from our previous work. “Preamble B” has been optimized by using random signal generation. The random signal generation repeats until its generated signal satisfactorily reduces the PAPR. As a result, “preamble B” reduced to 5.26 dB in PAPR.

3.3.2 Evaluation of RF-Baseband Simulation

We evaluated the non-linear amplifier performance using a baseband-RF simulation. The simulation model integrates both baseband and RF processing, such as using an OFDM transmitter and receiver, a power amplifier, and low-pass and band-pass filters. Table 5 lists the simulation conditions. The communication performance in a single-input single-output (SISO)-OFDM was tested for a multipath fading channel environment. Figure 12 shows the power amplifier model used in our simulation. The P1dB indicates an index of the output power performance where the amplifier

Fig. 12 Power amplifier model.

Fig. 13 Evaluation of BER performance in baseband-RF simulation.

characteristic displays 1-dB degradation from the ideal characteristic. This amplifier model has a maximum 30 dBm in output power. We evaluated the BER performance whose results are summarized in Fig. 13. We checked the output power values for the BER criterion of 10^{-3} for comparison. Their values depended on the types of modulations and preambles. When an output power value was larger, the communication distance could be elongated by increasing the transmitter power. Since the amplifier model assumes average values in input and output power, the amplifier back-off by a PAPR value must be considered so that the signals at the peak are not saturated by the non-linear characteristics. This indicates that the available output power for a satisfactory communications ($\text{BER} \leq 10^{-3}$) is decreased by the PAPR value. The output power value in “preamble A” and the “64-QAM R=3/4” is 14.8 dBm, which roughly corresponds to the subtraction of the maximum amplifier output power of 30 dBm to the PAPR value of 17.83 dB. The output power in “preamble B” and the “64-QAM R=3/4” is 26.1 dBm for a PAPR value of 5.26 dB. “Preamble B” causes a smaller back-off and provides a larger output power than “preamble A”. The 11.4-dBm difference between the

Fig. 14 RF transmitter and receiver architectures.

Fig. 15 Evaluation of BER performance in experimental platform.

two preambles corresponds to the more than three times extension of the communication distance.

3.3.3 RF Transceiver Fabrication and its Evaluation

Figure 14 shows the architectures of our RF transmitter and receiver. The parameters of the level diagrams are determined by our simulation in Sect. 3.3.2. The other parameters are based on those from the IEEE802.11a standard. The RF transmitter and receiver were fabricated and embedded into the RF unit shown in Fig. 6 (a). We evaluated the communication performance in the experimental platform by directly connecting the transmitter and receiver RF cables. The evaluation results are illustrated in Fig. 15. “Preamble B” in “64-QAM R=3/4” outperforms “preamble A” by 15.4 dBm in amplifier output power for a BER of 10^{-3} . This is similar to the RF-baseband simulation in Fig. 13.

4. Wireless Experiment

4.1 Experimental Condition

We evaluated the communication performance of our experimental platform in farm and passage environments. The experimental place and communication environments are shown in Fig. 16. The field experiment was executed on the Hokkaido University Sapporo Campus. We obtained an experimental radio license for the 5150–5250 MHz bands in Japan. In the experiment, we fixed the transmitter and moved the receiver to expand the distance between them. The experimental conditions are enumerated in Table 6. Directional receiver antennas were used to enhance the communication performance for the line-of-sight (LOS) channels. We tested QPSK, 16QAM, 64QAM with an 1/2-coding rate, and 64QAM with a 3/4-coding rate in modulation, whose modulation modes correspond to the 133, 266, 400, and 600 Mbps data rates in the PHY layer, respectively. The maximum transmit power per antenna was set to 24 dBm. The transmit power was decreased to 14 dBm for communication distances of 10, 20, and 40 meters to avoid saturation of the low noise amplifier (LNA) in the receiver.

4.2 Experimental Results

The evaluation results of the throughput performance are shown in Fig. 17. The passage environment has higher throughputs than the farm environment. The throughput values in the passage and farm environments do not decrease from 40 to 80 meters. This is caused by the increase in transmit power (i.e., 14 to 24 dBm) explained in Sect. 4.1. The received SNR values are plotted in Fig. 18. The same SNR values are observed at distances of 40 and 80 meters.

(a) Experimental Place

(b) Passage Environment

(c) Farm Environment

Fig. 16 Experimental place and communication environments.

We measured the MIMO channel characteristics from the received long training symbols in Fig. 4. The MIMO channel matrix and received SNR value are computed from the training symbols. The received SNR is given by a ratio of the measured signal power and noise power. The measured channel capacity of MIMO can be calculated from the MIMO channel matrix and SNR value [14]. We use the following equation for this:

$$C_{\text{MIMO}} = E \left[\frac{1}{K} \sum_{k=1}^K \log_2 \left(\det \left(\mathbf{I} + \frac{P}{\sigma^2} \mathbf{H}_k \mathbf{H}_k^H \right) \right) \right], \quad (1)$$

where $\mathbf{H}_k$ is the MIMO channel matrix with a k -th subcarrier matrix. P and σ^2 denote the received signal power and noise variance, respectively. K is the number of data subcarriers. Figure 19 shows the results of the measured channel capacity. The results show similar characteristics as those in the throughput performance. The passage environment has a higher channel capacity than the farm environment. Note that the MIMO channel capacity comes from the Shannon theory. It cannot estimate an actual throughput, which depends on the MIMO detection, error correction, channel equalization, etc. For instance, the theoretical throughput

Table 6 Experimental conditions.

Radio Frequency Band	5150 - 5250 MHz
Transmit Power per Antenna	14 dBm (10/20/40 m Distance) 24 dBm (80/160 m Distance)
TX Antenna (Directional)	NATEC PAT509S-4953 9 dBi / E-Plane 58 deg / H-Plane 76 deg
RX Antenna (Directional)	NATEC VA505A-W52 5 dBi / E-Plane 40 deg / H-Plane 360 deg
Channel	Line of Sight (LOS)
Sampling Rate in DAC/ADC	400 Msps
Communication System	2x2 MIMO-OFDM
OFDM Subcarrier Count	512
Data Subcarrier Count	408
Transmitted Signal Bandwidth	79.68 MHz
Modulation & Coding	QPSK, 16QAM, 64QAM
Coding	Convolutional Coding (Coding Rate 1/2, 3/4)
Error Correcting	Viterbi Decoding

Fig. 17 Evaluation of throughput performance.

Fig. 18 Evaluation of received SNR.

Fig. 19 Evaluation of channel capacity.

for a distance of 80 m and a passage environment is computed by $10.82 \text{ bps/Hz} \times 80 \text{ MHz} = 866 \text{ Mbps}$. This is far from the measured throughput of 256 Mbps. Despite this large difference, the ratios in the throughputs between the passage and farm environments (1.37 to 1.68) are similar to those in the channel capacity (1.47 to 1.62), excluding that for 160 meters. This fact indicates that the channel capacity can be used as a measure for comparing the throughput performances between communication environments.

The evaluation results of the eigenvalues, computed from the measured MIMO channel matrix, are presented in Fig. 20 for a distance of 80 m. The higher and lower eigenvalues are expressed as λ_1 and λ_2 , respectively. The lower eigenvalue in the farm environment is smaller than the one in the passage environment. The farm environment caused high MIMO channel correlations compared with that in the passage environment, which induced the degradation of the MIMO spatial separation. This phenomenon would similarly happen for the other channel bandwidths.

We measured the delay spread value under the condition that the power value of an impulse response is more than the noise floor of -30 dB . The delay spread values are plotted by the cumulative probability, which are shown in Fig. 21. The delay spread values in the passage and farm environments are 90 and 190 ns for a 90% cumulative probability. The maximum delay spread for a 100% cumulative

Fig. 20 Evaluation of cumulative probability in eigenvalues.

Fig. 21 Evaluation of cumulative probability in delay spreads.

probability was 260 ns.

5. Conclusion

This paper presents the development and outdoor evaluation of an experimental platform in a 2×2 MIMO-OFDM system for the wider channel of more than 80 MHz. The MIMO-OFDM transceiver has been designed to support a new OFDM system with an 80-MHz channel bandwidth and achieved real-time operation in MIMO detection. The experimental platform consists of the baseband and RF units. The RF transceiver has been designed based on our simulation results and showed enough RF performance in outdoor communication. We evaluated system performance in the experimental platform and investigated outdoor communication characteristics in the farm and the passage environments. The farm environment caused high MIMO channel correlation and degraded MIMO spatial separation performance. Further improvement of the experimental platform would be needed to cope with the degradation.

Our experiment was performed on the condition of line-of-sight (LOS). The measurement in non-line-of-sight (NLOS) conditions is left for our future work. In the NLOS conditions, communication performance is sensitive to locations where woods and buildings shade a direct radio path. We would like to find appropriate locations and investigate

their communication performance.

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