A Built-in Test Circuit for Electrical Interconnect Testing of Open Defects in Assembled PCBs

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SUMMARY In this paper, a built-in test circuit for an electrical interconnect test method is proposed to detect an open defect occurring at an interconnect between an IC and a printed circuit board. The test method is based on measuring the supply current of an inverter gate in the test circuit. A time-varying signal is provided to an interconnect as a test signal by the built-in test circuit. In this paper, the test circuit is evaluated by SPICE simulation and by experiments with a prototyping IC. The experimental results reveal that a hard open defect is detectable by the test method in addition to a resistive open defect and a capacitive open one at a test speed of 400 kHz.

1. Introduction

The electronic circuits discussed in this paper are made by soldering ICs to a printed circuit board (PCB). Such electronic circuits have been fabricated with fine pitch PCBs and fine IC chips for optimally miniaturizing. As a result, an open defect may occur at an interconnect between an IC and a PCB during the soldering process. In order to avoid a malfunction of the circuit, such defects must be detected prior to shipping. In this paper, we discuss how to detect an open defect in an assembled PCB and locate the defective interconnect.

BGA ICs have recently gained much popularity in the fabrication of electronic circuits. It is impossible to attach a test probe to input and output pins of a BGA IC. Thus, it is impossible for open defects occurring at interconnects between an IC and a PCB to be detected by providing a test signal to the IC and measuring an output signal with test probes. Also, it is impossible to visually examine connectivity between the IC and the PCB, as pins of the IC are located underneath the package.

In order to detect an open defect and locate the defective interconnect by visual inspection, X-ray inspection methods have been proposed [1], [2]. However, such test methods are rarely used in production tests, being prohibitively long and prone to creating false alarms for good interconnections.

In order to test an assembled PCB without attaching test probes, boundary scan test methods [3] have been proposed. Open defects that can generate logical errors are very effectively detected by such test methods. However, an open defect that can only generate small delay may not be detected by the test methods. Further, it takes a long time to locate the defective interconnect.

Open defects that cannot be detected by a boundary scan test method may be detected by testing an assembled PCB circuit electrically. Thus, electrical test methods have been proposed [4]–[11]. Test methods based on a time domain reflectometry (TDR) have been proposed to test an assembled PCB circuit [4]–[7]. However, it is difficult to realize robust tests, since high-frequency measurement is requested in the tests.

Capacitance between a land on a PCB and an IC pin appears whenever an open defect occurs. Thus, electrical test methods based on such capacitance effects have been proposed [8]. In order to enhance the testability for complex memory devices, a design-for-test method of an IC package is proposed [9]. When the land and the pin become disconnected by an open defect, it will be detected by the test method. However, if there are only partially connected, only a small delay occurs and the open defect may not be detected by the test method.

An electrical test method based on charging and discharging times of a capacitor that is added to a pin of a BGA IC has been proposed in [10], [11]. The test method is applicable only to interconnect tests of FPGA ICs.

Authors of this paper have proposed electrical test methods that are capable of both detecting an open defect as well as locating the defective interconnect [12]. Furthermore, we have proposed a built-in test circuit so that interconnects between BGA ICs and a PCB can be tested by the test method [13]. An inverter gate is used as a sensor for detecting an open defect in the test circuit. The test method is based on measuring the supply current of the inverter gate flowing when a time-varying voltage signal is provided to a targeted interconnect. We have shown by SPICE simulation that an open defect which does not generate a logical error can also be detected by the test method [13].

The built-in test circuit is made of analog switches and a switch control circuit. An AC signal is supplied to a tar-
geted interconnect through one of the switches. The analog switches can be replaced by MOS switches. Size of the built-in test circuit may be reduced by the replacement. In an attempt to make the size of a built-in test circuit as small as possible, we have revised the built-in test circuit. Also, we propose how to determine test signals for detecting open defects with the test circuit. The new built-in test circuit and the test signal generation method are described in Sect. 2.

We examined testability with the test circuit by SPICE simulation and by experiments. The testability analysis results are included in Sect. 3.

2. Electrical Interconnect Test by a Built-in Test Circuit

2.1 Built-in Electrical Test Circuit

ICs and PCBs that are used for fabrication are tested fully prior to soldering. Thus, it is assumed in this paper that there are no defects in them. An open defect at an interconnect between a land on a PCB and an IC pin may occur during the soldering process. Examples of the open defects are illustrated in Fig. 1.

An interconnect is divided into two parts by an open defect. When the space between the disconnected interconnect sides is large, no logical signal can be transferred. Such open defect is denoted a “hard open defect” in this paper. An open defect open#1 in Fig. 1 is a hard open one that is caused by missing a solder ball. The defective interconnect is modeled as a resistor of an infinite resistance.

When the gap space is small, a high speed signal may pass through. The defect is denoted a “capacitive open defect” in this paper. A capacitive open defect is generated by a large crack in a solder ball shown as an example as open#2 in Fig. 1 [11]. The defective interconnect is modeled as a capacitor.

A finite resistance of an interconnect becomes possible as generated by a partially open defect. Additional propagation delay is caused by such a resistance. The defective interconnect is built by a void or a small crack in a solder ball [11] and modeled as a resistor. The defect is denoted a “resistive open defect” in this paper. An open defect open#3 in Fig. 1 is a resistive open one.

This paper proposes an electrical test method and a built-in test circuit to detect these three kinds of open defects. The built-in test circuit is depicted in an IC $ICA$ of Fig. 2.

The built-in test circuit is made of a test control circuit block $TCB$, a switch block $SB$ and an open sensor block $OS$. In the test circuit, an inverter gate is used as a sensor detecting an open defect. An inverter gate is implemented as an element of a buffer gate between an input protection circuit and the core logic circuit in an IC. It is used as a sensor.

Electrical characteristics of an inverter gate are shown in Fig. 3. As shown in Fig. 3, whenever the input voltage of the inverter gate $V_i$ is in a range of either a high ($H$) or a low ($L$) level signal, no supply current flows. On the other hand, when $V_i$ satisfies Eq. (1), large supply current flows, as both a pMOS $Pa$ and an nMOS $Na$ in the gate turn on.

$$V_{i1} \leq V_i \leq V_{i2} \quad (1)$$

where $V_{i1}$ is the minimum voltage of $V_i$ for $Na$ to be on and $V_{i2}$ is the maximum voltage of $V_i$ for $Pa$ to be on. These are depicted in Fig. 3 (b).

Input voltage of the inverter gate in a defect-free PCB circuit is in a range of either a $H$ or a $L$ level signal and little to no supply current flows in the gate. On the other hand, when an open defect occurs in the PCB circuit, the input voltage of the gate may be in the range defined by Eq. (1). In this case, large supply current will flow into the gate. We detect the open defect by means of the abnormal current that is measured external to the circuit under test (CUT).

However, when an open defect occurs at an input terminal of an IC, the input voltage may not be in the range that may allow an excessive current detection. In order to shift the voltage to the needed range during our tests, a built-
in test circuit consisting of TCB, SB and OS is embedded within each of the ICs in a CUT.

In our tests, two kinds of supply source voltages are provided to ICs in a CUT as shown in Fig. 2. The one is \( V_{DDS} \) for input/output circuits and our test circuits in the ICs. The other is \( V_{DDC} \) for core circuits in them. We test a PCB circuit by measuring supply currents of the input and output circuits and of our test circuits. In case of a CUT in Fig. 2, we test it by measuring supply current \( i_{DDS} \) from \( V_{DDS} \).

TCB is a shift register with two control signals. The length of the register equals the number of input signal lines of the IC. The following interconnects are not targeted by the test circuit: \( V_{DDS}, V_{DDC} \) and \( V_{SS} \). One of the control signals is a test mode signal \( TM_i \) and the other is a reset \( RST \). The register is synchronized with a clock signal \( TCK \). All of the D-FFs in the TCB are initialized by \( RST \) whereas all of the nMOSs in SB are turned off. Hence, logic signals provided to the input pins are propagated to the inverter gates in OS. In a normal mode of the PCB circuit, input signals are provided after \( RST \).

\( TM_i \) is a signal for selecting either a test mode or a normal mode. When a positive pulse \( TM_i \) is not provided to an IC, input interconnects of the IC are not tested.

An operation of TCB is demonstrated in Fig. 4. As shown, after a positive pulse \( TM_i \) is provided to TCB, one of the nMOSs in SB is turned on by an output signal from TCB. Thereafter, a time-varying test input signal \( T_{sig} \) is provided to an interconnect through the nMOS. The interconnect is called in this paper a “targeted interconnect”, since it is tested by turning on the nMOS switch.

\( T_{sig} \) is generated by a \( T_{sig} \) generator that is denoted as “\( T_{sig Gen.} \)” in this paper. The generator is made of a resistor \( R_s \), a DC voltage source \( V_T \) and an AC voltage source \( V_S \) as shown in Fig. 2. \( T_{sig} \) is defined by Eqs. (2) and (3).

\[
T_{sig} = V_T + V_S \tag{2}
\]

\[
v_S = V_S \sin(2\pi f_s t) \tag{3}
\]

where \( V_S \) and \( f_s \) are fixed amplitude and frequency of \( v_S \), respectively.

2.2 Electrical Test Method

Whenever an assembled PCB circuit made of ICs that embed the test circuit described in this paper, is tested by the described test method, \( T_{sig}, RST, \) and \( TCK \) are provided to all of the ICs in the PCB circuit as shown in Fig. 2.

In the tests, only one of the nMOS switches in SB within the IC is turned on by an output signal from TCB. Waveforms of the input voltage of an inverter gate \( INV_{A1} \) in Fig. 2, \( v_{INV_{A1}} \), whose input terminal is connected to a turned-on nMOS switch, are shown in Fig. 5. In case of a defect-free circuit, when a \( L \) level signal is provided to the targeted interconnect \( a \) in Fig. 2 by providing a \( L \) level signal to \( PI_1 \), \( v_{INV_{A1}} \) is in the range of a \( L \) level signal, since it is pulled down by the driver gate. Thus, large \( i_{DDS} \) will not flow. If an open defect occurs at the targeted interconnect, \( v_{INV_{A1}} \) may become larger than that of the defect-free circuit, since it may not be pulled down by the driver gate. When it is in the range defined by Eq. (1), large \( i_{DDS} \) will flow from \( t_1 \) to \( t_2 \) as shown in Fig. 5 (a). When a \( H \) level signal is provided to the targeted interconnect in the defect-free circuit, \( v_{INV_{A1}} \) is pulled up by the driver gate and is in the range of a \( H \) level signal. If an open defect occurs at the targeted interconnect, \( v_{INV_{A1}} \) can become small, since it is not pulled up by the driver gate. Thus, as shown in Fig. 5 (b), when it is in the range defined by Eq. (1), large \( i_{DDS} \) will flow from \( t_3 \) to \( t_4 \).

By using the above phenomenon, if measured \( i_{DDS} \) satisfies Eq. (4) in our tests, we judge that an open defect occurs at a targeted interconnect.

\[
i_{DDS} \geq I_{th} \tag{4}
\]

where \( I_{th} \) is a threshold value. Theoretically, \( I_{th} \) is the max-
Fig. 6 Test environment in our tests.

Fig. 7 Current paths in the tests for a resistive interconnect $b$.

Fig. 8 Equivalent circuits illustrated in the tests of Fig. 7.

An assembled PCB circuit made of more than one testable designed IC is tested in a daisy chain style. In order to test the circuit, an output signal $T Mo$ of one testable designed IC is transferred to an input terminal of $T Mi$ in a succeeding IC as shown in Fig. 2. In case of the PCB circuit, input interconnects of $IC B$ are tested after ones of $ICA$, since $T Mo$ of $ICA$ is propagated as $T Mi$ of $IC B$.

A test environment in our tests is shown in Fig. 6 for testing the CUT of Fig. 2. An open defect occurring at an output terminal of an IC is detected as an open defect at an input terminal of a succeeding tested IC. Thus, we test a PCB circuit by examining whether Eq. (5) is satisfied.

Open defects occurring at $R S T$, $T C K$, $T Mi$ and $T Mo$ are detected by measuring the current flowing through $R S$. The current will change in time when an nMOS of $S B$ is turned on. If no change appears in the tests, it is determined that an open defect occurs at an interconnect of the signals.

Only one interconnect other than $R S T$, $T C K$, $T Mi$ and $T Mo$ is tested at a time in our tests. Thus, a defective interconnect can be located by examining which nMOS switch in $S B$ is turned on when an elevated $i D D S$ flows.

2.3 Test Input Signals

The following parameters, that are called “test parameters” in this paper, should be specified prior to conducting the tests: $V S$, $V T$, $f s$, and $R S$. This subsection proposes how to specify these parameters.

When a circuit is tested, $i D D S$ flows to a circuit that consists of (a) a $T s i g$ generator, (b) an output circuit block in a driver IC that is made of an output protection circuit and an output buffer gate, and (c) an input circuit block in a receiver IC that is made of an nMOS switch of $S B$, an inverter gate connecting to the nMOS, and an input protection circuit. An example of the circuit is shown in Fig. 7. In that circuit, a resistive open defect of $R f$ occurs at an interconnect $b$ between $IC#1$ and $IC#2$ in the circuit. When a hard open defect occurs at the interconnect, $R f$ is removed from the circuit. When a capacitive open defect occurs at the interconnect, $R f$ is replaced by a capacitor $C f$.

The test parameters should be derived so as for Eq. (4) not to be satisfied in tests of a defect-free circuit, and be satisfied in any one of the defective types, respectively.

When a $H$ level signal is provided to both $b$ and an nMOS switch $N S$ in a defective CUT, a supply current flows through a pMOS $P 1$ in the output buffer to the $T s i g$ generator along a current path $Path#1$. The equivalent circuit is shown in Fig. 8(a). In the circuits, $R P l o n$ and $R N o n$ are
on-resistances of $P1$ and $N_S$, respectively. $R_{pro}$ is a resistor in the input protection circuit. $V_{INV2}(H)$ appears when a $H$ level signal is provided to $b$, which is the input voltage of the inverter gate connecting to $N_S$ and defined by Eq. (6).

$$V_{INV2}(H) = \frac{(R_S + R_{Non})(V_{DDS} - V_T - V_S)}{R_S + R_{Non} + R_{pro} + R_f + R_{Pf1}}$$  
(6)

When a $L$ level signal and a $H$ level one are provided to $b$ and $N_S$ in the defective CUT, respectively, current flows from the $T_{sig}$ generator to an nMOS $N1$ through $N_S$ along a current path $Path#2$ as shown in Fig. 7. The equivalent circuit is shown in Fig. 8 (b). In that circuit, $R_{Inv}$ is the on-resistance of $N1$. $V_{INV2}(L)$ appears when a $L$ level signal is provided to $b$, which is the input voltage of the inverter gate connecting to $N_S$, and is defined by Eq. (7).

$$V_{INV2}(L) = \frac{(R_{pro} + R_f + R_{Non})(V_T + V_S)}{R_S + R_{Non} + R_{pro} + R_f + R_{N1on}}$$  
(7)

A large $I_{INV}$ in Fig. 8 should flow in the defective circuit. Thus, when a $H$ level signal is provided to $b$, the minimum value of $V_{INV2}(H)$, $V_{INV2}(H)_{min}$, should be smaller than $V_{th2}$. When a $L$ level signal is provided to $b$, the maximum value of $V_{INV2}(L)$, $V_{INV2}(L)_{max}$, should be larger than $V_{th1}$. Thus, both Eqs. (8) and (9) should be satisfied.

$$V_{INV2}(H)_{min} \leq V_{th2}$$  
(8)

$$V_{INV2}(L)_{max} \geq V_{th1}$$  
(9)

where $V_{INV2}(H)_{max}$ and $V_{INV2}(L)_{max}$ are defined by Eqs. (10) and (11), respectively.

$$V_{INV2}(H)_{min} = \frac{(R_S + R_{N1on})(V_{DDS} - V_T - V_S)}{R_S + R_{Non} + R_{pro} + R_f + R_{Pf1}}$$  
(10)

$$V_{INV2}(L)_{max} = \frac{(R_{N1on} + R_{pro})(V_T + V_S)}{R_S + R_{Non} + R_{pro} + R_f + R_{N1on}}$$  
(11)

A hard open defect is modeled as an infinite resistance $R_f$. Thus, $V_{INV2}(H)$ and $V_{INV2}(L)$ are obtained by removing $R_f$ from the equivalent circuits in Fig. 8. No current will flow from and to the $T_{sig}$ generator in the defective circuit. Thus, $V_{INV2}(H)$ and $V_{INV2}(L)$ are identical to $V_T + V_S$. A large $I_{INV}$ flows when Eq. (1) is satisfied. Therefore, the minimum value of $T_{sig}$ should be less than $V_{th2}$ and the maximum value of $T_{sig}$ should be greater than $V_{th1}$. That is, both Eqs. (12) and (13) should be satisfied.

$$V_T - V_S \leq V_{th2}$$  
(12)

$$V_T + V_S \geq V_{th1}$$  
(13)

When a capacitive open defect of $C_f$ occurs at $b$, the equivalent circuits are altered by replacing $R_f$ with $C_f$. Since the same phenomena happen as when a hard open defect occurs at the interconnect, it is detected by $V_S$, $V_T$, $f_s$, and $R_0$ that are specified to detect a hard open defect. $V_{INV2}(H)$ and $V_{INV2}(L)$ in a defect-free circuit are derived by replacing $R_f$ in Eqs. (6) and (7) with a short circuit. Eqs. (14) and (15) should be satisfied, since large $I_{INV}$ should not flow in case of a defect-free circuit.

$$V_{INV2a}(H)_{min} > V_{th2}$$  
(14)

$$V_{INV2a}(L)_{max} < V_{th1}$$  
(15)

where $V_{INV2a}(H)_{min}$ and $V_{INV2a}(L)_{max}$ are the minimum value of $V_{INV2a}(H)$ and the maximum value of $V_{INV2a}(L)$ in the defect-free circuit, respectively. These are defined by Eqs. (16) and (17).

$$V_{INV2a}(H)_{min} = \frac{(R_S + R_{Non})(V_{DDS} - V_T - V_S)}{R_S + R_{Non} + R_{pro} + R_f + R_{Pf1}}$$  
(16)

$$V_{INV2a}(L)_{max} = \frac{(R_{N1on} + R_{pro})(V_T + V_S)}{R_S + R_{Non} + R_{pro} + R_{N1on}}$$  
(17)

When $b$ is not selected as a targeted interconnect, $N_S$ is turned off by providing a $L$ level signal to the gate terminal. In this case, either a $H$ or $L$ level signal will be propagated from the frontier gate and a large $I_{INV}$ will not flow.

$V_S$, $V_T$ and $R_f$ should be specified so as for either Eqs. (14) and (15), or Eqs. (8), (9), (12) and (13) to be respectively satisfied in a defect-free CUT or defectives. However, it is impossible to specify the resistance range of $R_f$ to be detected that satisfies Eqs. (8) and (9) before deriving the parameters, since it depends on $R_f$ whether Eqs. (8) and (9) are satisfied. At the least, the parameters should satisfy the equations from Eq. (12) to Eq. (15). Thus, we derive the parameters to only satisfy the equations for a defect-free circuit and for a defective one occurring due to a hard open defect in Fig. 8.

Since $R_{Pf1}$, $R_{N1on}$ and $R_{pro}$ being nonlinear resistors are difficult to specify, we derive the parameters by SPICE simulation for the circuit shown in Fig. 9 performing DC sweep analysis varying $V_{TST}$ from 0V to $V_{DDS}$. $R_3$ used to prevent a CUT destruction by the test and voltage sources must be specified first. Resistive open defects of small resistance can be detected by using a small resistance $R_s$. Thus, $R_f$ should be as small as possible. However, since it is not permitted for a large output current to flow at an output terminal in an IC, Eq. (18) should be satisfied in the tests.

$$I_{omin} \leq I_b \leq I_{omax}$$  
(18)

where $I_{b}$ is the current flowing through $b$, and $I_{omin}$ and $I_{omax}$ are the minimum and the maximum currents that can flow through an output pin of IC#1.
When a defect-free circuit is tested by our test method, $I_d$ is identical to the current through $R_S$ that is referred to as $I_{TST}$ in this paper. $R_S$ should be specified so that $I_{TST}$ can be in the range specified in Eq. (18). Thus, we derive the maximum current and the minimum current through $b$ by performing a DC sweep analysis for the circuit in Fig. 9 with $R_S = 0\, \Omega$ varying the supply voltage from 0 to $V_{DDS}$, when a $H$ level signal is provided to $b$ and when a $L$ level signal is provided to it. $R_S$ is specified so that these can be in the range of Eq. (18).

After specifying $R_S$, in order to derive $V_S$ and $V_T$ for tests in which a $H$ level signal is provided to $b$, we perform a DC sweep analysis of the circuit by changing $V_{TST}$ with a switch $SW_1$ connected to side 2. From the simulation results, the minimum value of $V_{TST}$, $V_{TST_{min}}$, is derived with which $I_{INV}$ in Fig. 9 becomes smaller than $I_{th}$ so as for Eq. (14) to be satisfied. It satisfies Eq. (19), since when $V_{TST_{min}}$ is provided to the circuit in Fig. 9, $I_{TST}$ flows into the $T_{sig}$ generator.

\[ V_{TST_{min}} < V_{th2} \]  
\[ (19) \]

Also, in order to derive the parameters for tests in which a $L$ level signal is provided to $b$, a DC sweep analysis is performed for the circuit by changing $V_{TST}$ with $SW_1$ connected to side 1. From the simulation results, the maximum value of $V_{TST}$, $V_{TST_{max}}$, is derived with which $I_{INV}$ becomes smaller than $I_{th}$ so as for Eq. (15) to be satisfied. It satisfies Eq. (20), since when $V_{TST_{max}}$ is provided to the circuit in Fig. 9, $I_{TST}$ flow from the $T_{sig}$ generator.

\[ V_{TST_{max}} > V_{th1} \]  
\[ (20) \]

$V_T$ and $V_S$ are determined from $V_{TST_{min}}$ and $V_{TST_{max}}$ by Eqs. (21) and (22), respectively, so that both of Eqs. (19) and (20) can be satisfied.

\[ V_T = (V_{TST_{max}} + V_{TST_{min}})/2 \]  
\[ (21) \]
\[ V_S = (V_{TST_{max}} - V_{TST_{min}})/2 \]  
\[ (22) \]

$V_T$ and $V_S$ determined by Eqs. (21) and (22) satisfy Eqs. (12) and (13), since $V_{TST_{max}}$ and $V_{TST_{min}}$ satisfy Eqs. (19) and (20). It means that they satisfy Eq. (12) through Eq. (15).

Ideally, $f_s$ may be identical to the frequency of $TCK$. When an nMOS switch is turned on, $T_{sig}$ is provided to an interconnect. However, there are some variations in the propagation delay times of $T_{sig}$ and $TCK$ to ICs in a CUT. Thus, an nMOS switch may not be turned on when the input voltage of an inverter gate in $OS'S$ is in the range of Eq. (5). Even if variations exist, the nMOS switch should be turned on. Thus, $f_s$ is specified so that more than one sine waveform can be provided within one period of $TCK$. The testing time depends on $f_s$. It is required to be as short as possible. Therefore, twice the frequency of $TCK$ is used as $f_s$ in our tests as shown in Fig. 4. It means that the testing time of an IC that has $N_i$ input signals is $N_i/(2f_s)$.

A large leakage supply current flows into a deep sub-micron CMOS IC in operation. Most of the current flows into a core circuit in the IC, since the core circuit is made of a large number of gates. In our tests, a CUT is tested by measuring $i_{DDS}$ that flows from $V_{DD}$ to $V_{DDS}$. Thus, leakage current in $i_{DDS}$ is not so large and open defects in a CUT made of a deep sub-micron CMOS IC are detected by our test method.

However, there can be a large number of input/output pins in a BGA IC. As the number of input/output pins becomes large, the total size of our test circuits becomes large and a large leakage supply current may flow from $V_{DD}$ to $V_{DDS}$ of the IC. Hence, change of $i_{DDS}$ from the defect-free CUT may not be buried by the large leakage current. In order to detect open defects in a CUT made of the IC by our test method, more than one $V_{DD}$ pin is added to the IC so that leakage current supplied from each of the $V_{DD}$ pin can become small. If $i_{DDS}$ of a $V_{DD}$ pin satisfies Eq. (4), it is determined as defective.

3. Evaluation by SPICE Simulation

Test input signals of our test method depend on input and output protection circuits inside ICs used in a CUT. Many semiconductor foundries do not provide details of the protection circuits. NXP Co. Ltd publish input and output protection circuits in an SSI library. Thus, a simulation circuit for this research was built with the SSI library and the test circuit was evaluated in detail by SPICE simulation. The evaluation results are denoted in 3.1.

It is indispensable to evaluate it experimentally with a real IC. Thus, we designed an IC in which our test circuit was embedded, and evaluated it with the prototype IC. The experimental evaluation results are denoted in 3.2.

3.1 Evaluation by SPICE Simulation

The testability of the electrical interconnect test method with the built-in test circuit has been verified by SPICE simulation. A two input OR gate IC is designed in which the built-in test circuit is implemented. In the design, a SPICE netlist is coded that includes an input protection circuit, an output protection circuit and logic gates from the SSI library of 74HC type distributed by NXP Co. Ltd. A shift register made of D-FFs in $TCB$ is designed along with the logic gates. The voltage of $V_{DD}$ and $V_{DDC}$ is taken to be 3.3 V.

A SPICE netlist of a CUT, $CUT#1$, is coded as shown in Fig. 10. A circuit block $CB$ that is made of a parasitic resistor $R_p$ and a parasitic capacitance $C_p$, is added to each of the signal lines between the two ICs. The following typical parameters for a BGA IC were used in the simulations: $R_p = 0.1\, \Omega$, $C_p = 10\, \mu F$ based on common engineering practices.

$R_S$ is specified from the maximum current that is derived from a DC sweep analysis of the supply from 0 V to 3.3 V of the circuit of $R_S = 0\, \Omega$ shown in Fig. 9. The analysis results revealed a maximum current of 7 mA. The maximum permissible output current of 74HC SSI’s is 25 mA. Thus, $R_S = 0\, \Omega$ is acceptable. However, a large current along $Path#1$ in Fig. 7 may flow into the voltage sources $V_T$
and $v_s$ during the tests. Thus, in our evaluation, we selected a resistor of 10 $\Omega$ as $R_s$.

We code a SPICE netlist of a circuit in Fig. 9 made of an input and output protection circuits, inverter gates in input and output buffer gates, and the nMOS switches that are identical to the ones in CUT#1 for specifying $V_T$ and $V_s$. DC Sweep analysis simulation results for the circuit are shown in Fig. 11. Since $i_{DDS}$ of a pico ampere order of magnitude flows in the defect-free circuit, a small current of that order could conceptually be used as $I_{th}$ in Eq. (4). However, testing by measuring $i_{DDS}$ of a pico ampere order of magnitude is a very challenging albeit not really necessary task. Thus, we derived $V_{TST_{min}}$ and $V_{TST_{max}}$ by setting $I_{th} = 1.5$ $\mu A$ in this evaluation.

From Fig. 11 (a), when a $H$ signal is provided to b in Fig. 9, $V_{TST}$ should be greater than 1.2 V. From Fig. 11 (b), when a $L$ signal is provided to it, it should be less than 1.6V, implying that $V_{TST_{min}}$ and $V_{TST_{max}}$ are 1.2 V and 1.6 V, respectively. Thus, the following parameters are selected from Eqs. (21) and (22): $V_T = 1.4$ V, $V_s = 0.2$ V.

The test signals shown in Fig. 4 are provided to CUT#1. A hard open defect, a resistive one and a capacitive one are inserted to an interconnect denoted as “A” in Fig. 10. A hard open defect is modeled by inserting a resistor of 1$G$ $\Omega$ at the interconnect. Resistive open defects are emulated by inserting a resistor that may vary from 10 $\Omega$ to 1$k$ $\Omega$. In our evaluation, a solder ball of 0.75 mm diameter and a land of 0.60 mm diameter are assumed to form an interconnect between the IC and a PCB. When a missing solder ball occurs, the capacitance of the capacitive open defect is about 5$fF$. When a crack of 0.5$\mu m$ width occurs at the interconnect, the capacitance of the defect becomes about 5$\mu F$. Thus, a capacitor ranging from 5$fF$ to 5$\mu F$ is inserted at the interconnect in this evaluation.

Our simulation results for the defect-free circuit are shown in Fig. 12 for a test speed of 10 kHz. As shown in Fig. 12, large $i_{DDS}$ never flows in the defect-free circuit independently of output logic values of the interconnect A. The current value is always less than 0.5$\mu A$ and $I_{th} = 0.5$ $\mu A$.

A simulation result for the defective circuit is shown in Fig. 13, in which a hard open defect occurs at interconnect A. As shown in Fig. 13, an $i_{DDS}$ waveform depends on a logic signal provided to the targeted interconnect, but the differences are small. The hard open defect is detected by the test method, since $i_{DDS}$ greater than 350 $\mu A$ flows in the defective circuit when the voltage at $Q_2$ is in the range of a $H$ level signal.

Some of the simulation results are shown in Fig. 14. Resistive open defects greater than 42 $\Omega$ are detectable by the test method, since the elevated $i_{DDS}$ is larger than $I_{th} = 1.5$ $\mu A$ as shown in Fig. 14 (a) and Fig. 14 (b). On the other hand, the capacitive open defects inserted in our evaluation are all detectable by the test method. Examples of simulation results are shown in Fig. 14 (c) and Fig. 14 (d). As the capacitance of a capacitive open defect becomes smaller, large change in $v_{G2}$ appears and large $i_{DDS}$ flows as shown in Fig. 14 (c) and Fig. 14 (d). Consequently the input impedance of an inverter gate connecting to a defective interconnect becomes smaller as the capacitance becomes smaller. A missing solder ball causes small capacitance effect. Thus, a capacitive open defect created by a missing solder ball is easier to detect than a crack.

When a hard open defect occurs, no output logic signal
Fig. 14 Simulation results in defective CUT#1.

from IC#1 is propagated to IC#2 in CUT#1. It will be detected by logic tests as a stuck-at fault. The resistive open defect of 42Ω causes additional delay of 0.45 nsec. It means that a resistive open defect that can generate the additional delay is detectable by the test method. When a capacitive open defect less than 0.205 pF occurs, a H level signal is always propagated to IC#2 and it is detected by logic testing. When a capacitive open defect greater than or equal to 0.205 pF occurs, an output logic signal from IC#1 can be propagated to IC#2 without additional delay owing to the capacitive coupling. Thus, the capacitive open defects cannot be detected by logic testing. On the other hand, these are detected by the test method. Since a capacitive open defect of large capacitance is detected by the test method, it is expected that an open defect caused by a small crack in a solder ball can be detected by our test method.

In order to examine the test speed of our test method, we varied the frequency of TCK. A simulation result for a defective CUT featuring a hard open defect at a test speed of 2.5 GHz is shown in Fig. 15. As shown, the hard open defect is detected. However, it is not detected at a test speed greater than 2.5 GHz, since a switch control signal of Q2 is not outputted from the shift register. Thus, a circuit is to be tested at a test speed slower than 2.5 GHz with the BIST circuit.

3.2 Evaluation with a Prototype IC

This section provides experimental verification results. We designed a layout of a die with 0.18μm CMOS process of Rohm Co. Ltd and fabricated a prototype IC embedding in it our built-in test circuit. A layout of the circuit in our prototype IC is shown in Fig. 16. The core circuit in the IC is an inverter chain circuit of two stages.

An experimental circuit shown in Fig. 17 was made with our prototype IC. Two kinds of power supply voltages should be provided to the IC. The first is a supply voltage for input/output circuits that is denoted as VDDS in Fig. 17. The
other is a supply voltage for the core circuit in the IC that is denoted as $V_{DDC}$. The following supply levels specified by the CMOS process were provided in our experiments: $V_{DDSS} = 3.3$ V, $V_{DDC} = 1.8$ V. We used the following parameters in a $T_{sig}$ generator that satisfy Eqs. (12) and (13): $V_s = 0.5$ V, $V_T = 0.5$ V and $R_s = 10\Omega$.

We inserted a hard open defect, a resistive one and a capacitive one at the input interconnect of $Di1$ in Fig. 17 and measured waveforms of $i_{DDSS}$ with a current probe of Tektronix TCP312 and TCPA300. A hard open defect is inserted by eliminating the input signal line from the experimental circuit. A resistive open defect and a capacitive one are emulated by actually adding a resistor and a capacitor to $Di1$, respectively, as it is hard to intentionally create a BGA solder ball crack.

A shift register operation designed in the prototype IC is shown in Fig. 18. When a $H$ level signal of $TMi$ in the IC is provided, logic signals shown in Fig. 18 are outputted from output terminals of $S0, S1, S2$ and $S3$ of the shift register. When a logic signal of $TMi$ is a $L$ level one, a $L$ level signal continues to be outputted from the terminals. The operation of the shift register is not the same as the one in Fig. 4. However, the IC can be used for evaluating testability of the test method with the built-in test circuit. Only one nMOS switch is turned on by synchronizing with $TCK$. Thus, we have examined testability of our test method with the IC.

Measured waveforms in the experiments for a test speed of 10 kHz are shown in Fig. 19. As shown in Fig. 19, the inserted open defects are detected by the test method, since $i_{DDSS}$ flows in Figs. 19(b), 19(c) and 19(d) that is greater than that in Fig. 19(a).

In order to examine the test speed, $f_s$ is varied in the experiments. The waveforms in the test speed of 400 kHz for a defect-free circuit and a defective one of a hard open defect are shown in Fig. 20. As shown in Fig. 20, the hard open defect cannot be detected by the test method at the given test speed. However, the open defect cannot be detected in a test speed of faster than 500 kHz, since an elevated supply current cannot be measured.

The test speed is slower than the one in the SPICE simulation. It stems from the difference in parasitic resistance and capacitance of the input signal lines and in the CMOS design process between the prototype IC and the IC in Fig. 10. However, it is concluded that open defects can be detected by the test method at a test speed of at least 400 kHz.

3.3 Discussion

Additional circuits in our built-in test circuit are $TCB$ and $SB$. $TCB$ is a shift register. The number of shift register cells in an IC depends on the number of input signal lines. With the number of IC input signal line of $Ni$, the shift register is made of $Ni$ D-FFs and an AND gate.

Additional signals are $T_{sig}, TMi, TMo$ and $TCK$, since there is a reset signal available in the electronic circuit which can be used as $RST$. Our test method is based on supply current of $V_{DDSS}$. Generally, two kinds of supply voltages are provided to an IC. The first is for a core circuit in the IC and the other is for input and output buffer gates. When such an IC is used in a CUT, pin overhead of each IC is 4.

In case of deep sub-micron CMOS ICs, the pin overhead may be greater than 4, since more than one $V_{DDSS}$ pin is added as denoted in Sect. 2.3. There are a large number of pins in BGA ICs. Thus, the pin overhead will be accepted.

A D-FF and an AND gate are made of 32 MOS transistors and 6 MOS transistors in our design, respectively. Thus, in case of an IC with $Ni$ input signal lines, the area overhead is $6 + 32Ni$. It seems to be sufficiently small and widely accepted by designers.

Only one input interconnect of an IC is tested at a time by our test method. Open defects at output interconnects in an IC are detected as ones at input interconnects in the succeeding ICs. Thus, the total test time of a CUT is $(N_{inp} + N_{pout})/(2f_s)$, where $N_{pout}$ and $N_{inp}$ are the number of
primary output signals, the total number of input signals of ICs in the circuit, respectively.

The test speed will depend on a layout design in a circuit under test and a built-in test circuit design. A circuit may be tested at a test speed faster than 400 kHz by suitable optimization.

There are bi-directional interconnects in a PCB circuit. When a high impedance signal is outputted to a bi-directional interconnect, the same supply current will flow as when a hard open defect occurs at the interconnect. Thus, the defect-free circuit may be determined as defective by our test method. In order to test the interconnect, we should add a test control circuit to our built-in test circuit so that either $H$ or $L$ signal can be outputted to the targeted interconnect.

As a time-varying signal, only $v_S$ is provided to a CUT in test by the test method proposed in [13]. Open defects can be detected by our test method at a higher speed than by the test method proposed in [13]. By a time-varying signal of $V_T + v_S$, input voltage of an inverter gate $V_{INVA}$ can be in the range from $V_{I1}$ and $V_{I2}$ for a longer time than by only $v_S$, since the amplitude of $v_S$ in this test method is smaller than the one in the test method proposed in [13] and changing speed of the time-varying signal is slower than the one proposed in [13]. Thus, a larger $i_{DDS}$ will be made flow by the signal of $V_T + v_S$ than by only $v_S$ and more open defects are detected by the test method that the one proposed in [13].

Testability of our test method with our built-in test circuit depends on process variation in inverter gates used for open defect sensors. $V_{I1}$ and $V_{I2}$ in Fig. 3 will vary in a range owing to the process variation. Thus, $v_S$, $V_T$ and $R_S$ should be specified from the process variation in addition to the equations from Eq. (12) to Eq. (15). The effects on them caused by process variation are difficult to be estimated. If only a DC voltage $V_T$ is provided to the CUT, a large change in $i_{DDS}$ may not be generated by process variation. A time-varying signal of $V_T + v_S$ is provided to a CUT in our test method as a test signal. Open defects can be detected even if process variation is not estimated precisely, since input voltage of an inverter gate in $OS$ may be in the range from $V_{I1}$ and $V_{I2}$ by providing the time-varying signal. However, it has not been examined the effectiveness for process variation fully. It remains as future work to examine it in addition to development of a test control circuit for testing bi-directional interconnects and detailed examination of test speed of our test method.

4. Conclusions

A built-in test circuit is proposed in this paper to detect an open defect at an interconnect in an assembled PCB circuit by an electrical test method. Testability of open defects in a circuit made of ICs in which the built-in test circuit is implemented is examined by SPICE simulation and experimentally with a prototype IC. It is shown by simulation results that a hard open defect, a resistive open one causing an additional delay of 0.45 nsec and a capacitive one can be detected by the test method. Also, it is shown experimentally that such can be detected at a test speed of at least 400 kHz. A capacitive open defect is not detected by logic testing, but it can be detected by the test method. Furthermore, it is easy to locate defective interconnects. Thus, the built-in test circuit is effective for realizing high reliability of an assembled PCB circuit.

It remains as future works to examine test speeds of the test method more thoroughly and effects on testability from process variation in the built-in test circuit. Also, bi-directional interconnects may be detected by adding a test control circuit to the built-in test circuit. The development of the control circuit is also a future work.

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