Effect of Threshold Voltage Fluctuations on Stability of Inverter Circuit of MOS Current Mode Logic

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1. INTRODUCTION
With the recent advances in the areas of high-speed communication systems and high-performance microprocessors, the demand for high-speed VLSI circuits is on the rise. Conventional CMOS circuits suffer from increased power dissipation at high speeds because their dynamic power dissipation is directly proportional to the frequency of operation. MOS Current Mode Logic (MCML) is emerging as a promising logic style that dissipates less power at relatively high frequencies (>about 2 GHz) than the conventional CMOS logic. MCML operation frequency is over GHz and its signal amplitude is less than some 100 mV. It is therefore important to investigate the stability of MCML against fluctuations of the threshold voltage (Vth) of the transistors. In this study, the stability of MCML inverter against fluctuations of Vth of PMOS and NMOS has been studied in DC characteristic by using HSPICE simulations.

2. RESULTS AND DISCUSSION
An MCML inverter is shown in Fig. 1. Fig. 2 shows diagrams of the input and output waveforms of the MCML inverter with Vth fluctuation. The MCML inverter is designed to satisfy that \( \Delta V_B = 0 \). If the Vth fluctuate, the output waveform has the bias offset voltage \( \Delta V_B \) [see Fig. 2] as compared from input waveform. Figs. 3 and 4 show the stability of \( \Delta V_B \) for the Vth of transistors obtained by HSPICE simulations. Fig. 3 is the results of simulated \( \Delta V_B \) versus Vth of PMOS and Fig. 4 is the results of simulated \( \Delta V_B \) versus Vth of NMOS. The simulations were carried out based on the assumption that the Vth of MP1 and MP2 are Vthp, and the Vth of MN1, MN2 and MC1 are Vthn. The parameters of 0.18-\( \mu \)m CMOS transistors with \(|V_{th}| = 0.4 \) were used in the HSPICE simulations. As shown in Fig. 3, the Vthp fluctuation of 0.1 V induces change of \( \Delta V_B \) from -0.1 V to 0.1 V. Fig. 4 shows that Vthn fluctuation of 0.1 V induces change of \( \Delta V_B \) from -0.5 V to 0.5 V. The dependence of \( \Delta V_B \) on Vthn is thus found to be about five times larger than the one on Vthp, for the first time.

3. CONCLUSION
The stability of \( \Delta V_B \) of MCML inverter versus Vth was simulated using HSPICE. It was made clear that the stability of the Vth of NMOS is the key point for improving the stability of MCML inverter.

REFERENCES

![Fig. 1. Inverter circuit of the MCML](image_url)

![Fig. 2. Diagram of the MCML input and output waveforms with Vth fluctuation](image_url)

![Fig. 3. Simulated \( \Delta V_B \) vs. Vthp](image_url)

![Fig. 4. Simulated \( \Delta V_B \) vs. Vthn](image_url)